NASA Contractor Report 3120

A Study to Investigate the Chemical Stability of Gallium Phosphate Oxide/Gallium Arsenide Phosphide

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SUMMARY

The purpose of this program was to study and determine the chemical stability under bias-temperature stress of $GaPO_4/Ga_2O_3$ insulating and passivating layers thermally grown on $GaAs_{1-x}P_x$ semiconductors. An additional objective was to investigate dielectric fabrication procedures for improving oxide-semiconductor interface properties. Oxides were thermally grown in dry O_2 or steam on $GaAs_{1-x}P_x$ for phosphorus mole fractions x = 0.4, 0.5, and 0.7.

The elemental composition of the oxide was examined as a function of depth using ion microprobe mass analysis. Results indicate that the layers are arsenic-deficient through the bulk of the oxide and arsenic-rich near both the oxide surface and the oxide-semiconductor interface region. Phosphorus is incorporated into the oxide in an approximately uniform manner.

Capacitance-voltage characteristics of MIS structures displayed the deep depletion behavior typically observed with wide bandgap semiconductor devices. These characteristics also exhibited hysteresis effects indicative of electron trapping at the oxide-semiconductor interface. Post-oxidation annealing of the oxides in argon or nitrogen at temperatures near 700°C resulted in reduced C-V hysteresis effects and increased dielectric leakage current. These electrical effects are accompanied by a loss of arsenic near the surface of the oxide layers. Annealing at 450°C did not result in significant changes in electrical or compositional properties. The results of bias-temperature stressing experiments indicate that the major instability effects are due to changes in the electron trapping behavior. No changes were observed in the ion microprobe profiles following electrical stressing, indicating that the grown films are chemically stable under device operating conditions.

SECTION I

INTRODUCTION

This report describes work performed from September 14, 1977 to March 14, 1978 on NASA Contract No. NAS1-15101. The primary objective of this program was to study and determine the chemical stability under bias-temperature stress of $GaPO_4/Ga_2O_3$ insulating and passivation layers thermally grown on $GaAs_{1-x}P_x$ semiconductors. An additional objective was the improvement and optimization of the dielectric fabrication process to produce high-quality oxide layers as evidenced primarily by low interface state density and high dielectric strength.

Surface passivation insulators are used as barriers to environmental exposure to improve the stability and performance of semiconductor devices. Thermally grown SiO_2 has resulted in the highest quality passivation layers in the silicon technology; however, limited research has been performed to study the effectiveness of thermally grown native insulators as passivation layers for III-V compound semiconductors. Although many device applications require an extremely low dielectric/semiconductor interface state density, all semiconductor devices benefit from surface passivation insulators which act as a barrier to contamination and which decrease junction leakage currents.

Several material properties of GaAs and the alloy $GaAs_{1-x}P_x$, including high electron mobility, large bandgap, and low minority carrier lifetime, make these III-V compound semiconductors attractive for high-speed, high-temperature device applications. Many of these properties can be optimized for certain applications by proper selection of the phosphorus mole fraction, x. Therefore, development of a passivating dielectric for GaAsP surfaces will be useful, not only in GaAsP devices, but also in ultimately developing a suitable dielectric for use in GaAs and other III-V compound semiconductors.

Several methods have been investigated for forming native dielectrics on GaAs. These include thermal oxidation, anodic oxidation, and, recently, plasma oxidation. In general, most of these oxides have exhibited inferior electrical properties due to dielectric leakage, large interface state densities, and charge trapping in the oxide. Oxides grown using the anodic and plasma techniques require post-oxidation annealing treatments at high temperature for stabilization. In addition, these methods are not well suited to large-scale device production because of the oxide growth procedure.

The major difficulty associated with thermal oxidation is related to the high equilibrium vapor pressure of arsenic at elevated temperatures, which results in arsenic loss and nonstoichiometry at the oxide-semiconductor interface. Because of this arsenic loss, thermal oxidation of GaAs results primarily in the formation of crystalline β-Ga_2O_3, which does not have suitable dielectric and surface passivation characteristics.

Thermal oxide has previously been grown on $GaAs_{0.5}P_{0.5}$ (Reference 1) and electrical measurements on these films were used to determine an optimum growth process. Coerver (Reference 2) conducted a literature survey to determine the possible constituents of the insulator grown at 700°C. This study indicated that the only possible solid compounds which can form the dielectric are β-Ga_2O_3 (gallium oxide), $GaPO_4$ (gallium phosphate) and $GaAsO_4$ (gallium arsenate). Further experiments (Reference 2) indicated that the film is composed of (Ga_2O_3 + $GaPO_4$), or gallium-phosphate-oxide (GPO). These results further indicated that gallium phosphate is probably the major molecular constituent.

Some of the initial electrical results on MOS devices indicated that this phosphate-containing thermal oxide might prove more useful for application to III-V compound semiconductor devices than oxides composed mainly of crystalline β-Ga_2O_3. Such crystalline oxides result during thermal oxidation of GaAs, and are usually not acceptable for device applications because of high leakage currents or instabilities. Subsequently, more detailed work (Reference 3) indicated that certain electrical instabilities and hysteresis effects occurred in $GaAs_{0.5}P_{0.5}$ MIS capacitors. Therefore, further investigations were indicated to determine if these instability effects were associated with chemical changes in the insulator. Also, additional variations in the dielectric growth and anneal procedures were needed to improve the oxide and interface properties and reduce hysteresis effects. These investigations form the basis of this research program.

Section II of this report describes the procedures used to thermally grow a native dielectric on $GaAs_{1-x}P_x$. The fabrication of MIS capacitor structures utilizing these thermal oxides as the gate dielectric is also discussed in this section.

Section III describes the electrical characteristics of MIS capacitors. The results of capacitance-versus-voltage and current-versus-voltage measurements are presented and related to variations in the fabrication procedure.

The results of ion microprobe analysis of the dielectric composition is given in Section IV. A description of this analysis technique and its limitations is presented in this section. Elemental depth profiles of the dielectric are then presented and related to growth and anneal variations used in the fabrication process.

The chemical stability of the insulator is examined in Section V by comparing electrical characteristics and ion microprobe results both before and after bias-temperature stressing of the devices.

Finally, Section VI summarizes the results and concluding remarks are given regarding possible process improvements and the direction of future III-V oxide research.

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SECTION II

DIELECTRIC GROWTH AND MIS CAPACITOR FABRICATION

This section describes the thermal growth of insulators on $GaAs_{1-x}P_x$ and the procedures for fabricating MIS capacitor structures using these insulators as the gate dielectric. The electrical properties of these structures are discussed in a later section of this report.

Starting Material

The semiconductor material used in this study was n-type (Te-doped) epitaxial gallium arsenide phosphide ($GaAs_{1-x}P_x$) of <100> orientation. Material of varying phosphorus content (i.e., phosphorus mole fraction, x) was investigated to determine any major interface effects due to differences in the relative arsenic/phosphorus composition of the semiconductor. The mole fractions used were x = 0.4, 0.5 and 0.7. Major emphasis, however, was directed toward $GaAs_{0.5}P_{0.5}$, because most previous work had been performed with this particular alloy composition (References 1 and 3).

The epitaxial layers were grown by chemical vapor deposition on heavily doped n-type ($\rho \approx 0.003$ Ω-cm) gallium arsenide (GaAs) or gallium phosphide (GaP) substrates. A region of linearly graded phosphorus composition was grown between the GaAs substrate (GaP for x = 0.7) and $GaAs_{1-x}P_x$ epitaxial layer. The thickness of this region varied from 20 to 50 micrometers, depending on the particular growth run. This graded region is included to minimize lattice mismatch in the epitaxial layer. However, the remaining mismatch results in dislocation arrays and surface structure, as shown in the Nomarski contrast photomicrograph of Figure 1 and the surface scan of Figure 2. Although these arrays are present on the semiconductor surface, reflection electron diffraction patterns have indicated that the material is single crystal (Reference 3).

The impurity concentration of the semiconductor surface was determined by capacitance-voltage characterization of Schottky diodes. Donor concentrations determined from $1/C^2$ vs reverse bias voltage plots were in the range of $1 - 9 \times 10^{16}$ cm^{-3}. Some implications of lower impurity levels in the epitaxial layer will be discussed in a later section.

Dielectric Growth

Prior to introduction into the oxidation furnace, the samples were cleaned and degreased in trichloroethane, acetone, and deionized water. This

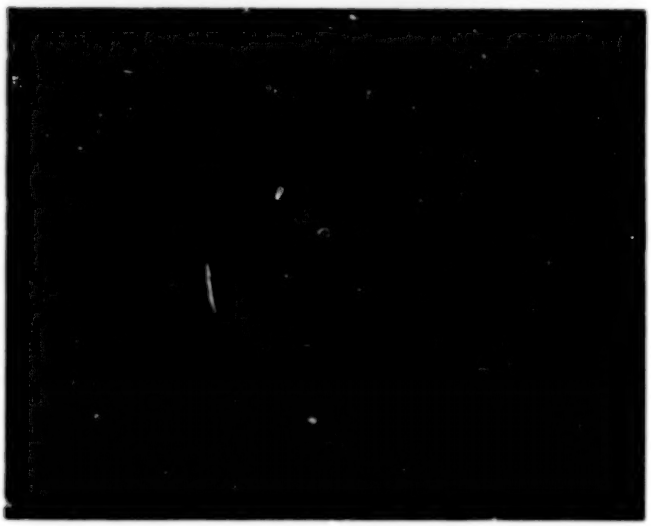


Figure 1. Nomarski Contrast Photomicrograph of $GaAs_{0.5}P_{0.5}$ Surface (97X)

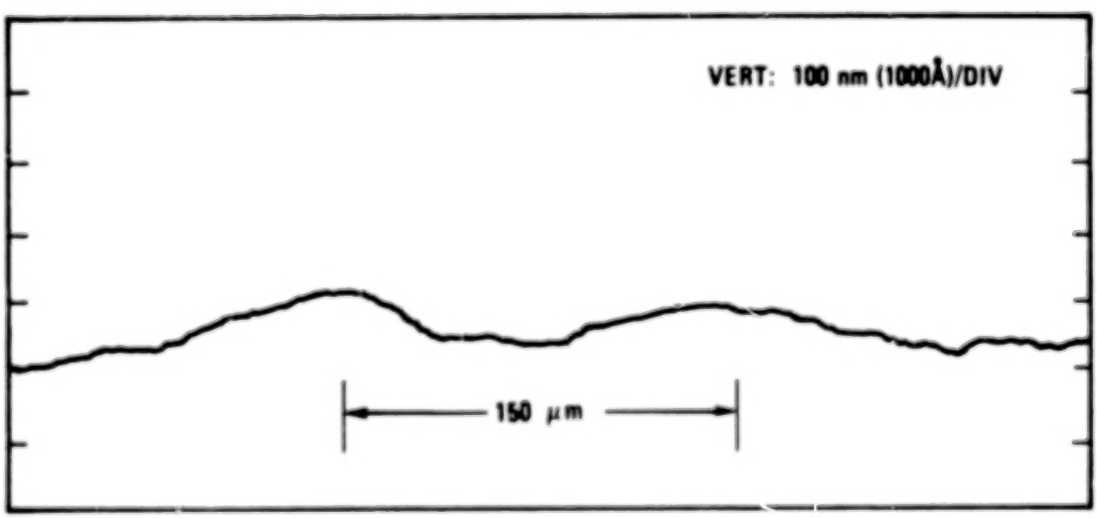


Figure 2. Surface Profile of $GaAs_{0.5}P_{0.5}$ Epitaxial Surface

procedure was followed by a chemical etch in $5H_2SO_4:H_2O_2:H_2O$ at room temperature for 5 minutes. This etching step removed approximately 2.5 μm from the epitaxial layer (Reference 4).

Various dielectric growth/anneal ambients and temperatures were investigated to determine the impact on interface properties. Oxidations were performed using either dry oxygen at 680°C (flow rate = 0.75 liter per minute) or steam at 600°C. Some of the dry oxides were annealed in either argon or nitrogen at 680°C or 450°C. All steam oxides were dried out or annealed in dry O_2 at 600°C for 120 min. Sometimes this annealing was followed by a second anneal in either N_2 or Ar at 600°C or 450°C. The gas flow rate during all annealing steps was one liter per minute.

Insulator thicknesses were determined by ellipsometry (@ 5640 Å) or step profiling following chemical etching in NH_4OH and $50H_2O:H_2SO_4:H_2O_2$ (Reference 3). The region of the insulator near the oxide surface is etched in room temperature NH_4OH at a rate of about 100 nm/min. This etching process stops before the oxide layer is completely removed. The thickness of the residual layer increases for increasing insulator thickness, and can be removed by a dip etch in $50H_2O:1H_2SO_4:1H_2O_2$ at room temperature. This procedure appears to remove the residual layer by attacking the underlying semiconductor surface. The amount of $GaAs_{1-x}P_x$ removed during this step is <35 Å.

The growth rate of oxide films grown on $GaAs_{0.6}P_{0.4}$ and $GaAs_{0.5}P_{0.5}$ in oxygen has been presented elsewhere (References 1 and 5). In general, most oxide layers in the present study were grown to a final thickness of 2000-2500 Å. This thickness required a growth time of 18-24 hours at 680°C in dry oxygen. A few preliminary experiments were conducted to demonstrate the feasibility of growing a lower temperature oxide using steam. Table I presents a comparison of the oxidation time, temperature and thickness for various films grown on $GaAs_{1-x}P_x$ in steam and dry O_2 during this investigation.

A discussion of the dielectric composition and the implications of the interfacial region will be given in a later section.

MIS Capacitor Fabrication

MIS capacitors were formed with aluminum vacuum evaporated through a metal shadow mask. The thickness of the aluminum gates were either in the

Table I. Comparison of Oxide Growth on $GaAs_{1-x}P_x$ in Dry Oxygen and Steam

Substrate	Ambient	Temp. (°C)	Oxidation Time (minutes)	Approx. Oxide Thickness (nm)
$GaAs_{0.5}P_{0.5}$	Steam	650°C	90	700
$GaAs_{0.5}P_{0.5}$	Steam	600°C	45	125
$GaAs_{0.5}P_{0.5}$	Dry O_2	700°C	370	118
$GaAs_{0.5}P_{0.5}$	Dry O_2	680°C	1200	200
$GaAs_{0.6}P_{0.4}$	Steam	550°C	60	10
$GaAs_{0.6}P_{0.4}$	Steam	550°C	180	41
$GaAs_{0.6}P_{0.4}$	Steam	550°C	360	200
$GaAs_{0.6}P_{0.4}$	Dry O_2	680°C	1200	230
$GaAs_{0.3}P_{0.7}$	Dry O_2	680°C	1200	150

80-200 nm (800-2000 Å) range or 1 μm. Thinner aluminum was used for samples undergoing ion microprobe analysis, and thicker metal was used for samples undergoing various electrical characterization.

No probe damage effects were noted using the thinner gate metal. Gate electrode areas were variable due to mask bowing and shadowing; therefore, the area of each device analyzed was measured using a filar microscope attachment.

Residual oxide formed on the GaAs substrate during oxidation was removed by mechanical lapping with 5 μm-alumina. Indium was then soldered onto the substrate and pulse-alloyed to form ohmic substrate contacts. A cross-section of the completed $GaAs_{1-x}P_x$ MIS structure is shown in Figure 3.

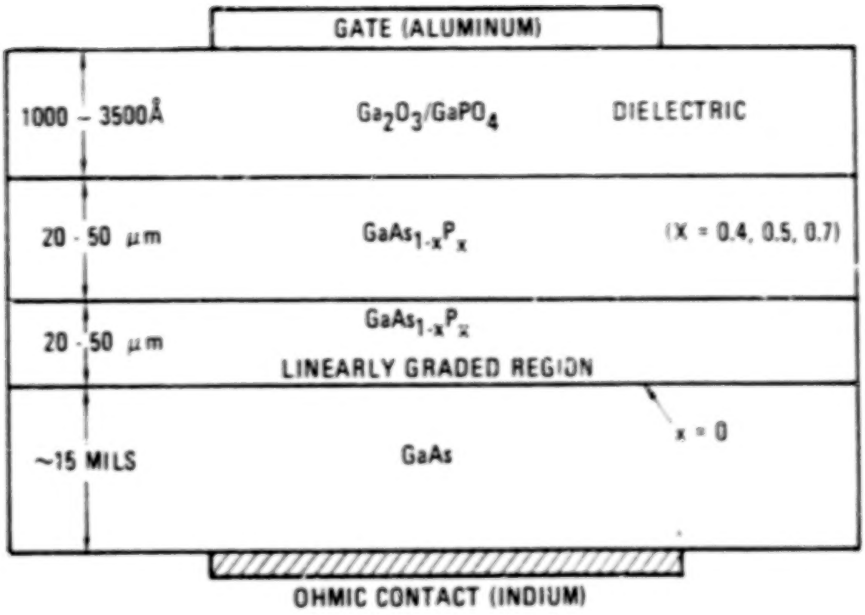


Figure 3. $GaAs_{1-x}P_x$ MIS Capacitor Structure

SECTION III

$GaAs_{1-x}P_x$ MIS CAPACITOR ELECTRICAL CHARACTERISTICS

This section describes the electrical and interface characteristics of $GaAs_{1-x}P_x$ MIS capacitors fabricated with a thermally grown gate dielectric. High-frequency capacitance-versus-voltage characteristics are presented, as well as the results of current-versus-voltage measurements. The results of bias-temperature stressing on electrical characteristics will be presented and related to ion microprobe results in a following section.

Capacitance-Versus-Voltage and Current-Versus-Voltage Characteristics

The main evaluation of interface characteristics was made through high-frequency capacitance-versus-voltage (C-V) measurements. Most measurements were performed at a frequency of 1 MHz using a Boonton Model 71A capacitance meter. Additional devices were characterized at different frequencies using a PAR Model 124 lock-in amplifier. No changes in the C-V characteristics (i.e., dispersion or accumulation capacitance values) were observed with frequency, as described earlier (Reference 3). This behavior is contrary to that reported for most GaAs anodic oxides (References 6 and 7), but similar to that reported for GaP anodic oxides (Reference 8).

Figures 4 through 6 illustrate the type of C-V characteristics observed for $GaAs_{0.6}P_{0.4}$, $GaAs_{0.5}P_{0.5}$, and $GaAs_{0.3}P_{0.7}$ MIS structures which had gate oxides grown for 20 hours in dry oxygen at 680°C. Included in these figures are the characteristics of devices from this same growth run but which underwent a post-oxidation argon anneal for 2 hours at 680°C.

The C-V characteristics exhibit depletion-type characteristics at room temperature as a consequence of the wide bandgap and low minority carrier generation rate and/or high dielectric leakage current.

The hysteresis observed in the C-V curves is similar to that observed previously on $GaAs_{0.5}P_{0.5}$ (Reference 3), GaAs (Reference 6), and GaP (Reference 8) MIS devices. The magnitude of the hysteresis depends on both the maximum bias applied during the sweep, and the bias sweep rate. In all of the experimental plots presented here, the device was biased at the maximum sweep bias (both positive and negative) for two minutes before sweeping or re-sweeping.

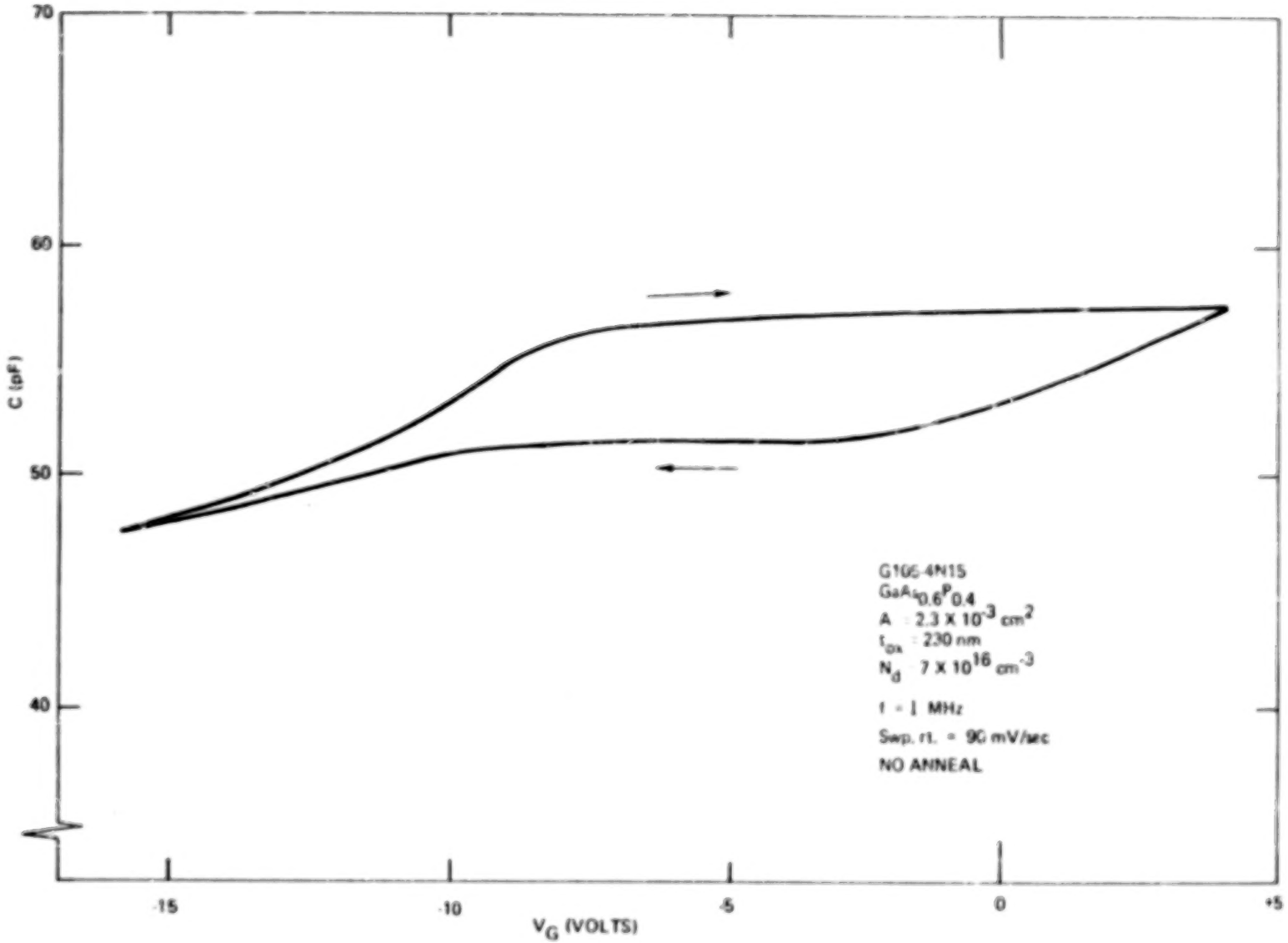


Figure 4(a). $GaAs_{0.6}P_{0.4}$ MIS C-V Characteristic--Unannealed

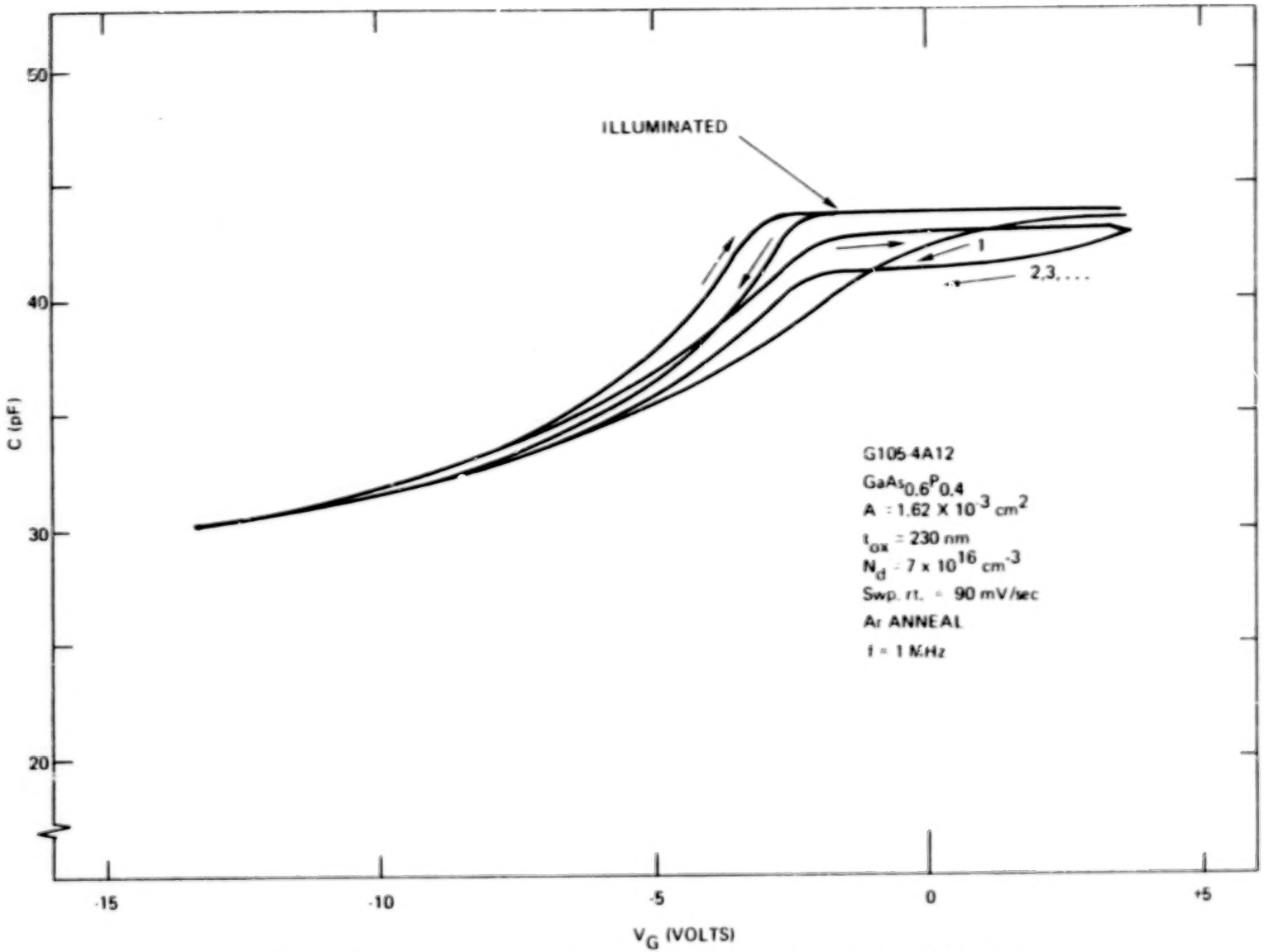


Figure 4(b). $GaAs_{0.6}P_{0.4}$ MIS C-V Characteristic:Ar-Annealed, 680°C, 2 Hr.

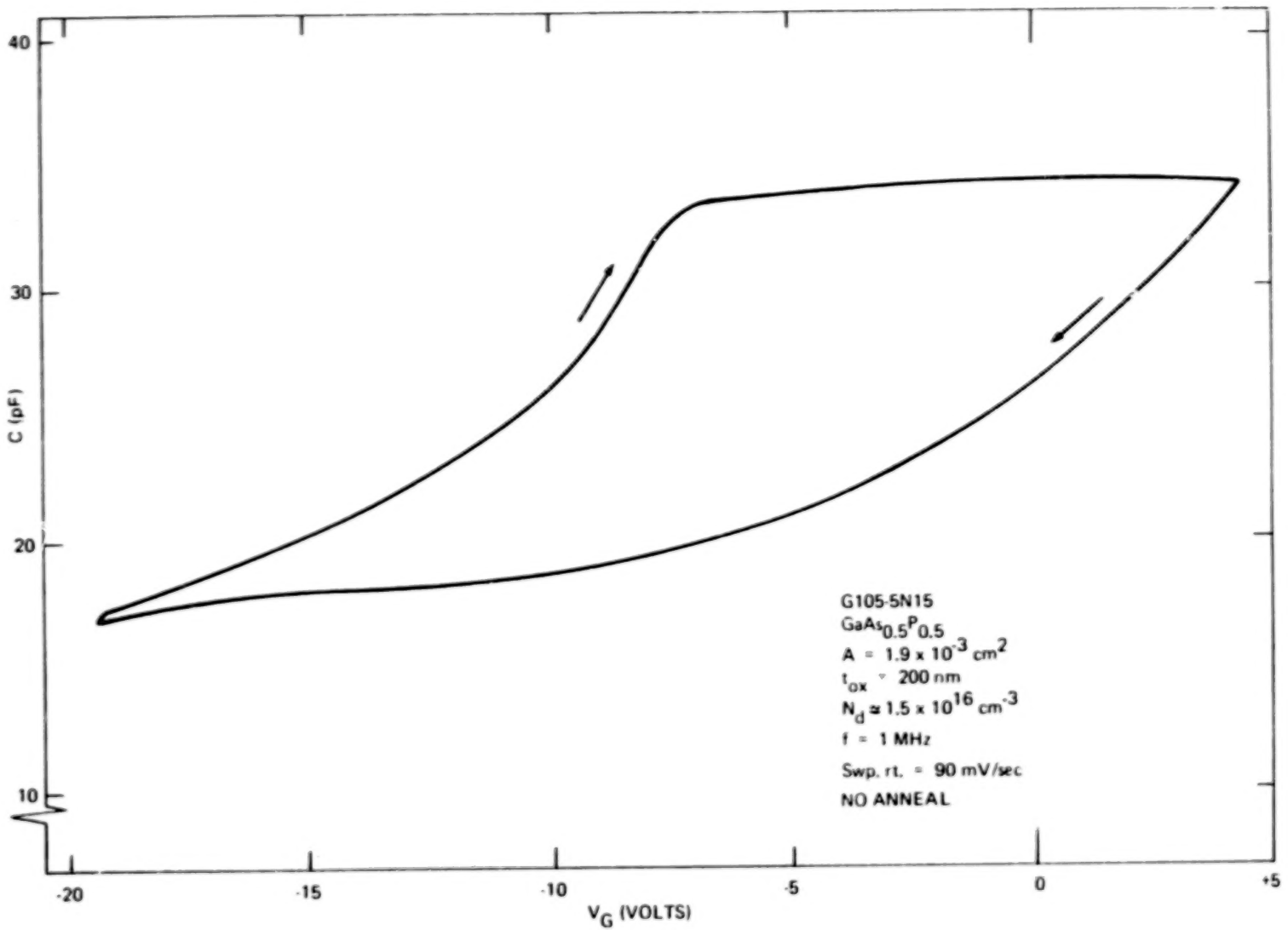


Figure 5(a). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristic--Unannealed

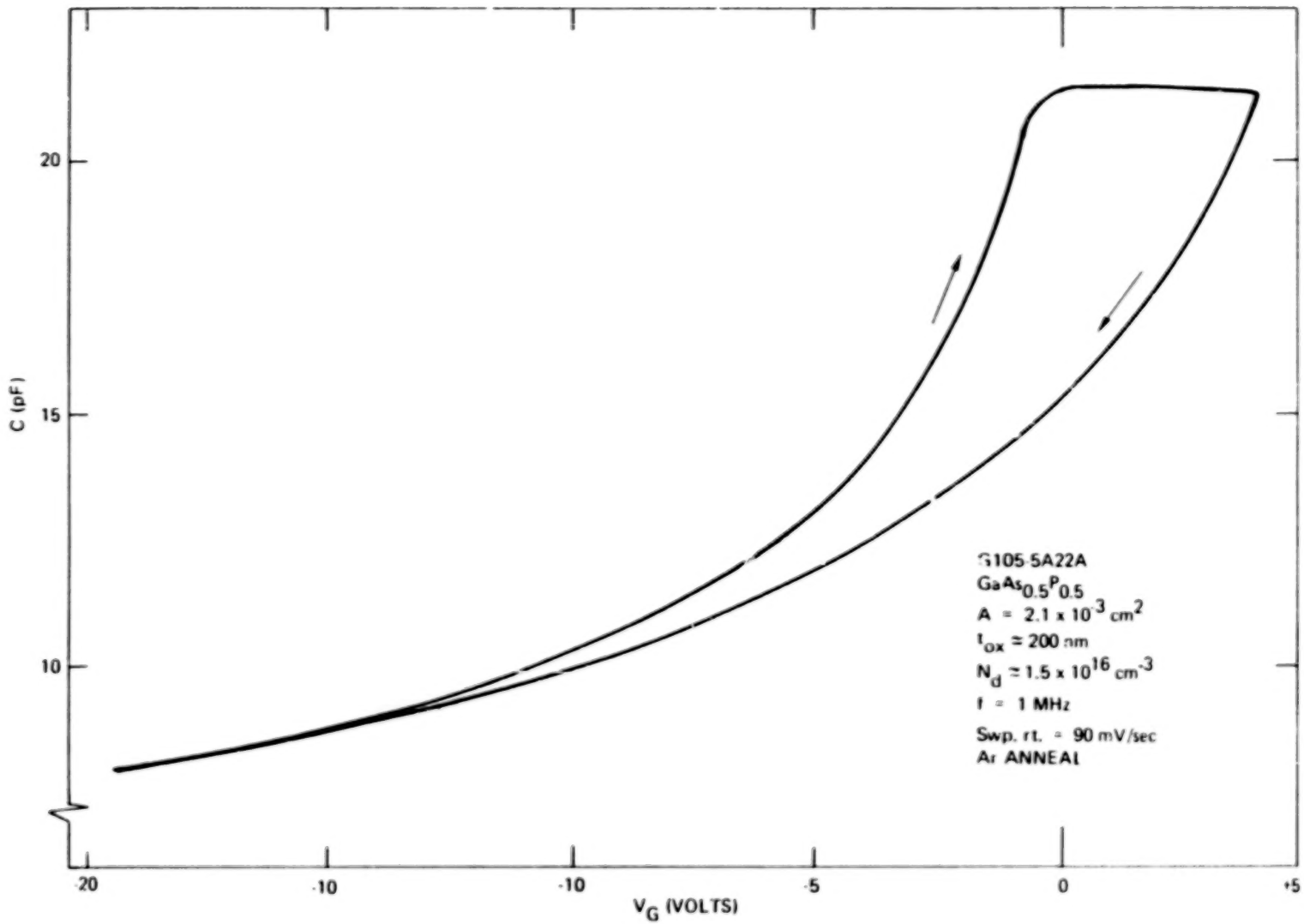


Figure 5(b). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristic:Ar-Annealed, 680°C, 2 Hr.

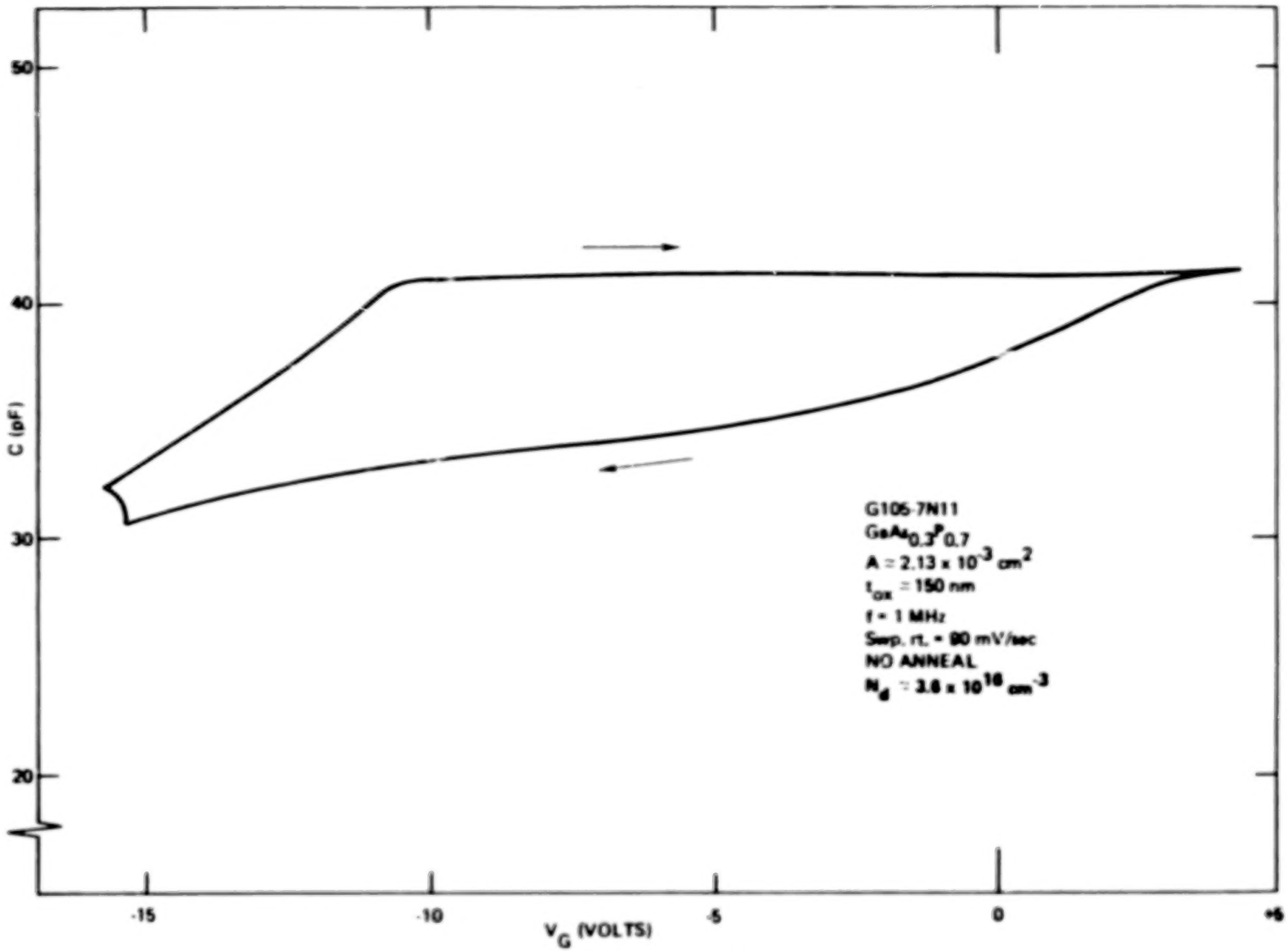


Figure 6(a). $GaAs_{0.3}P_{0.7}$ MIS C-V Characteristic--Unannealed

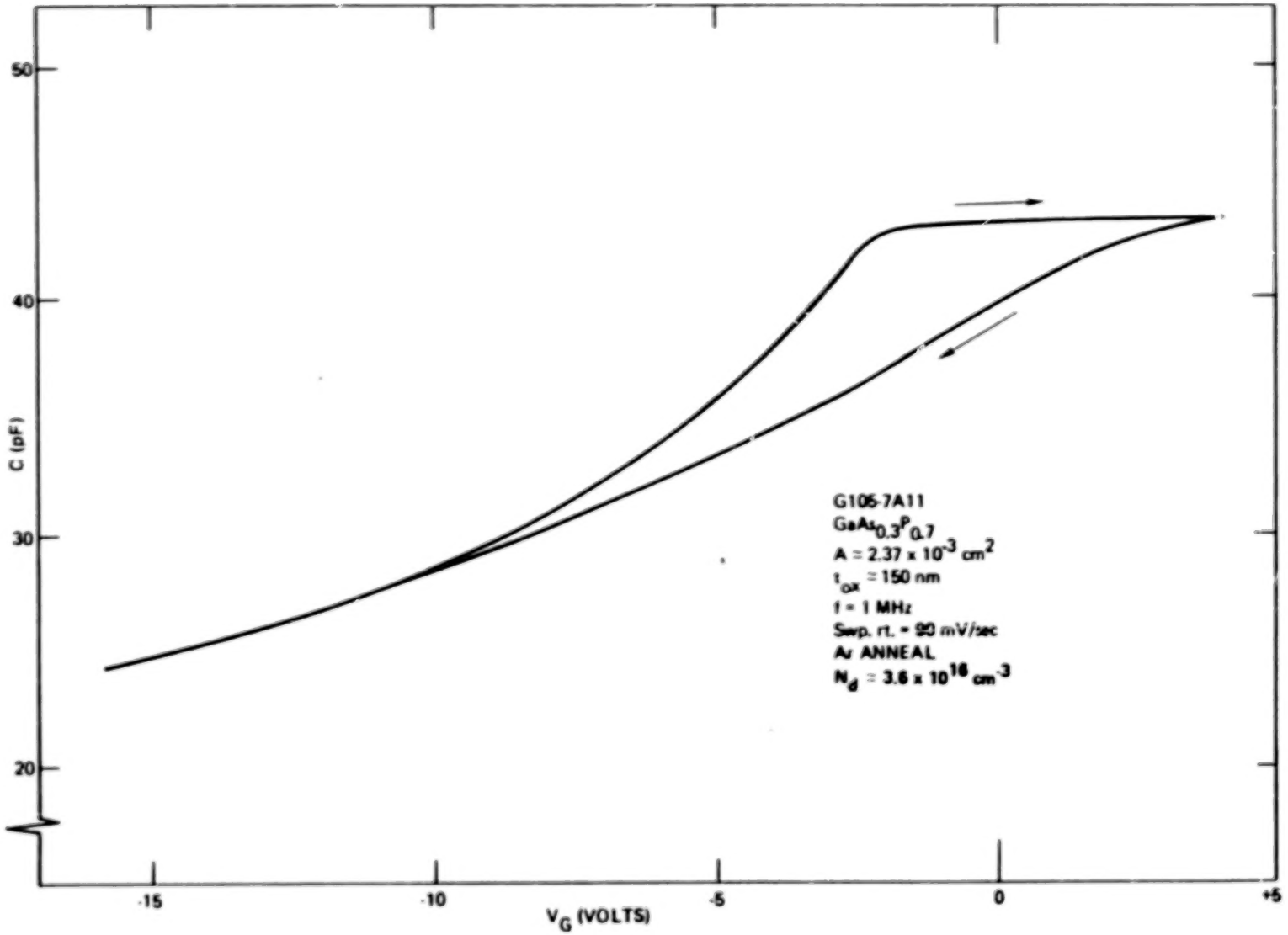


Figure 6(b). $GaAs_{0.3}P_{0.7}$ MIS C-V Characteristic:Ar-Annealed, 680°C, 2 Hr.

Hysteresis Effects -- The hysteretic behavior of these devices is apparrently due to electron injection and trapping in the oxide near the oxide-semiconductor interface. The large amount of hysteresis in MIS devices fabricated on widegap semiconductors, such as $GaAs_{1-x}P_x$ ($1.43 \leq E_g \leq 2.25$ eV for $0 \leq x \leq 1$), can be attributed to the fact that the emission rate of the electron traps is too low for them to follow the dc voltage variation during the sweep (Reference 9). Illumination with white microscope light (~10 mW cm^{-2}) removes a large part of the hysteresis by increasing the trap emission rate, as shown in Figure 4(b).

Comparison of Figures 4(a), 5(a) and 6(a) shows that the amount of trapping induced voltage shifts in the unannealed device does not vary significantly for the various mole fractions. These voltage shifts correspond to approximate equivalent trapped charge densities of 1-2 x 10^{12} cm^{-2} at flatband.

The major effect of annealing in argon at 680°C is to decrease the amount of hysteresis in the C-V characteristics. This decrease is generally accompanied by an increase in the dielectric leakage current, of less than an order of magnitude, as shown in Figure 7 for the $GaAs_{0.6}P_{0.4}$ devices of Figure 4. Somewhat larger increases in leakage have been noted previously after nitrogen anneal (Reference 3).

Annealing also reduced the dielectric breakdown strength of the insulators. Breakdown occurred when the leakage current reached a current density of about 1 mA/cm^2. Breakdown measurements were made by "walking-out" the I-V characteristic to avoid large transient currents due to trap filling and emptying. Dielectric breakdown strengths ranged from about 9 x 10^5 V/cm for nitrogen annealed oxides to about 2 x 10^6 V/cm for unannealed oxides. Ar-annealed films had dielectric strengths intermediate to these values.

Figures 8(a) - (c) illustrate the effect of lower temperature post-oxidation annealing on the C-V hysteresis. These devices had oxides grown in dry O_2 at 680°C for 26 hours. The growth was then followed by annealing at 450°C for 30 minutes in either O_2, N_2, or Ar. There is no significant difference in hysteresis between devices with argon and oxygen anneal. Nitrogen annealing, however, results in increased oxide leakage current beginning at +2 volts which, in turn, results in reduced hysteresis [Figure 8(b)].

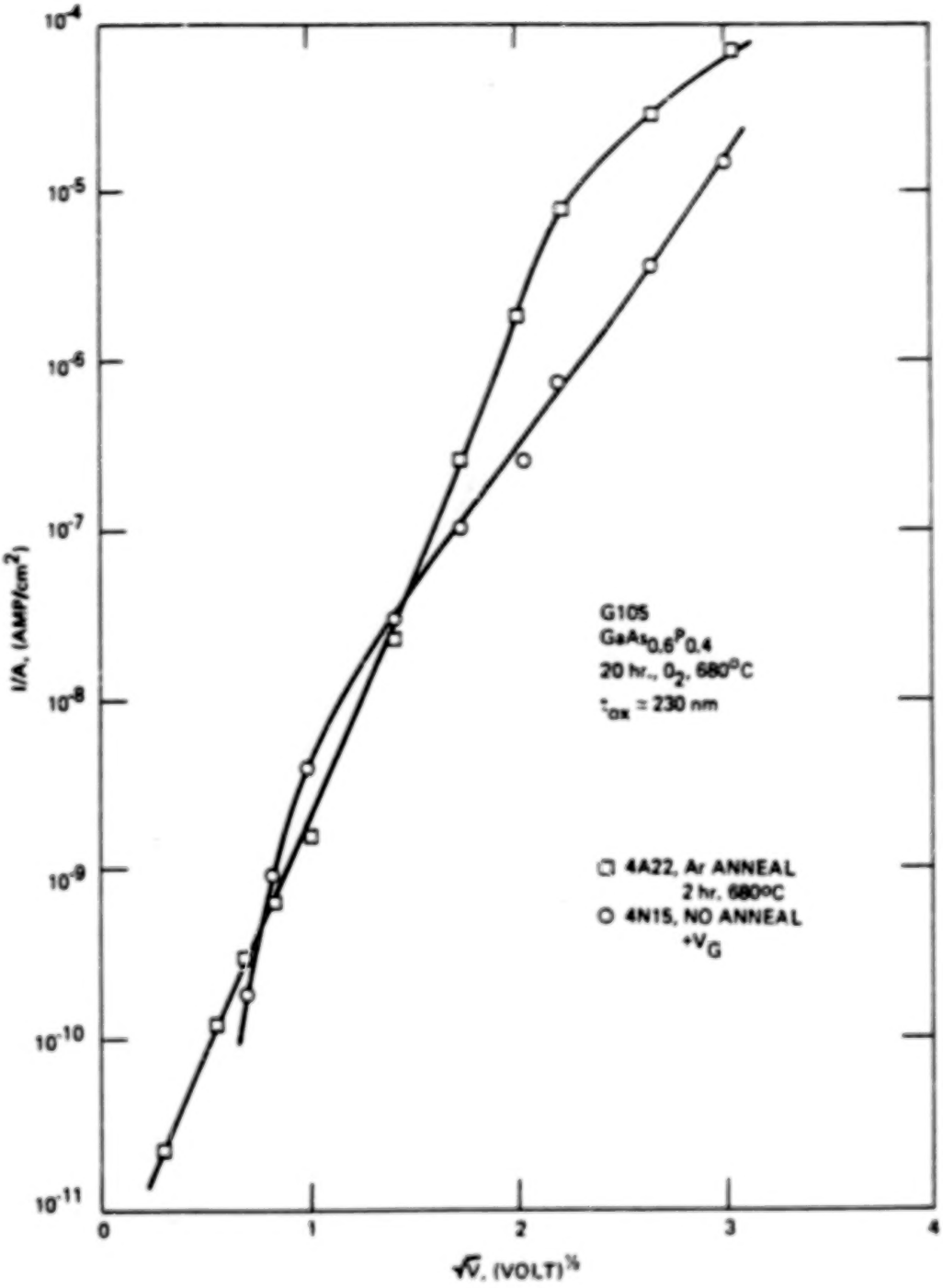


Figure 7. Comparison of Ar-Annealed and Unannealed $GaAs_{0.6}P_{0.4}$ I-V Characteristic

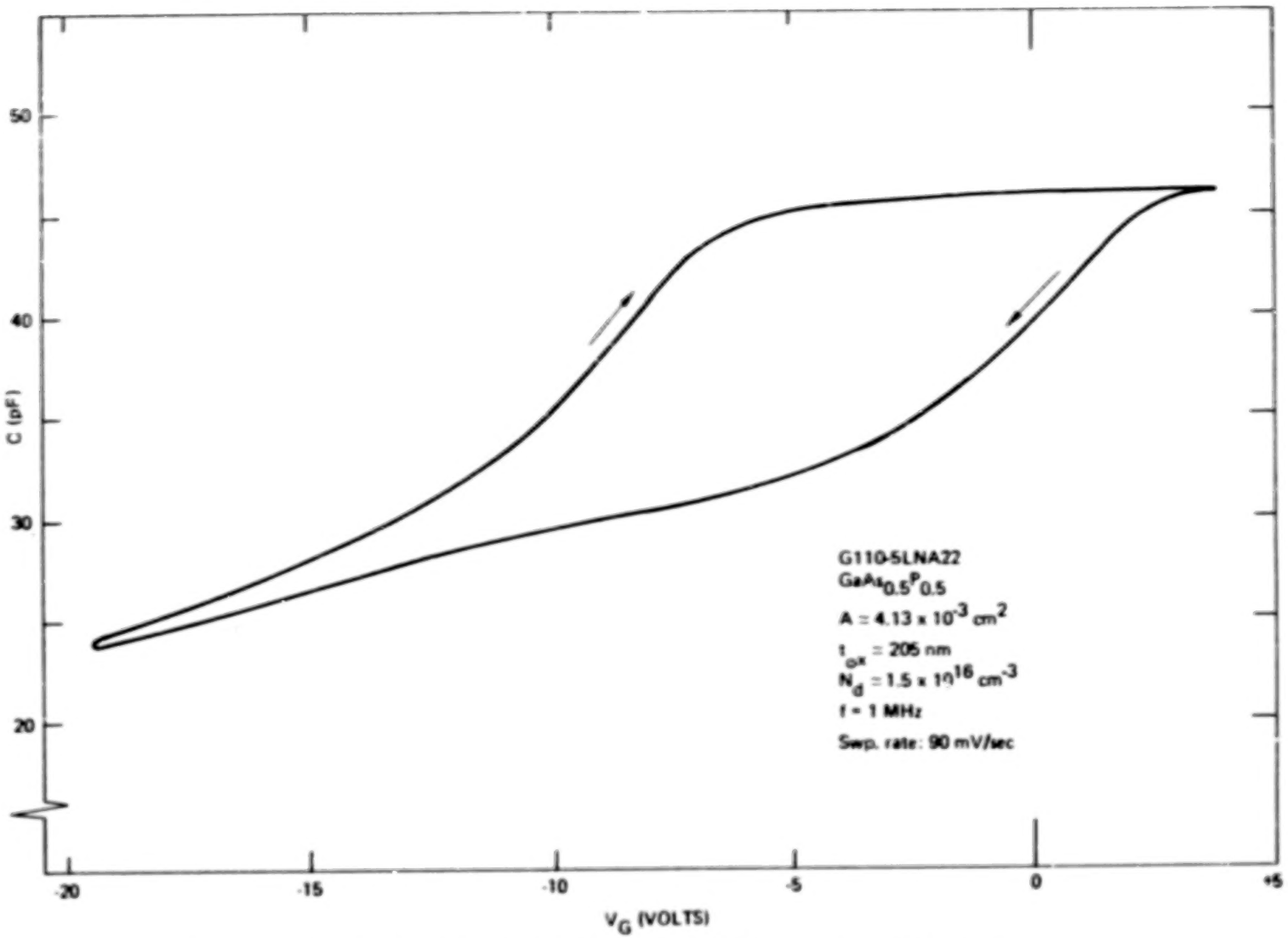


Figure 8(a). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristics for Dry Oxides Grown at 680°C, O_2 Anneal, 30 Min., 450°C

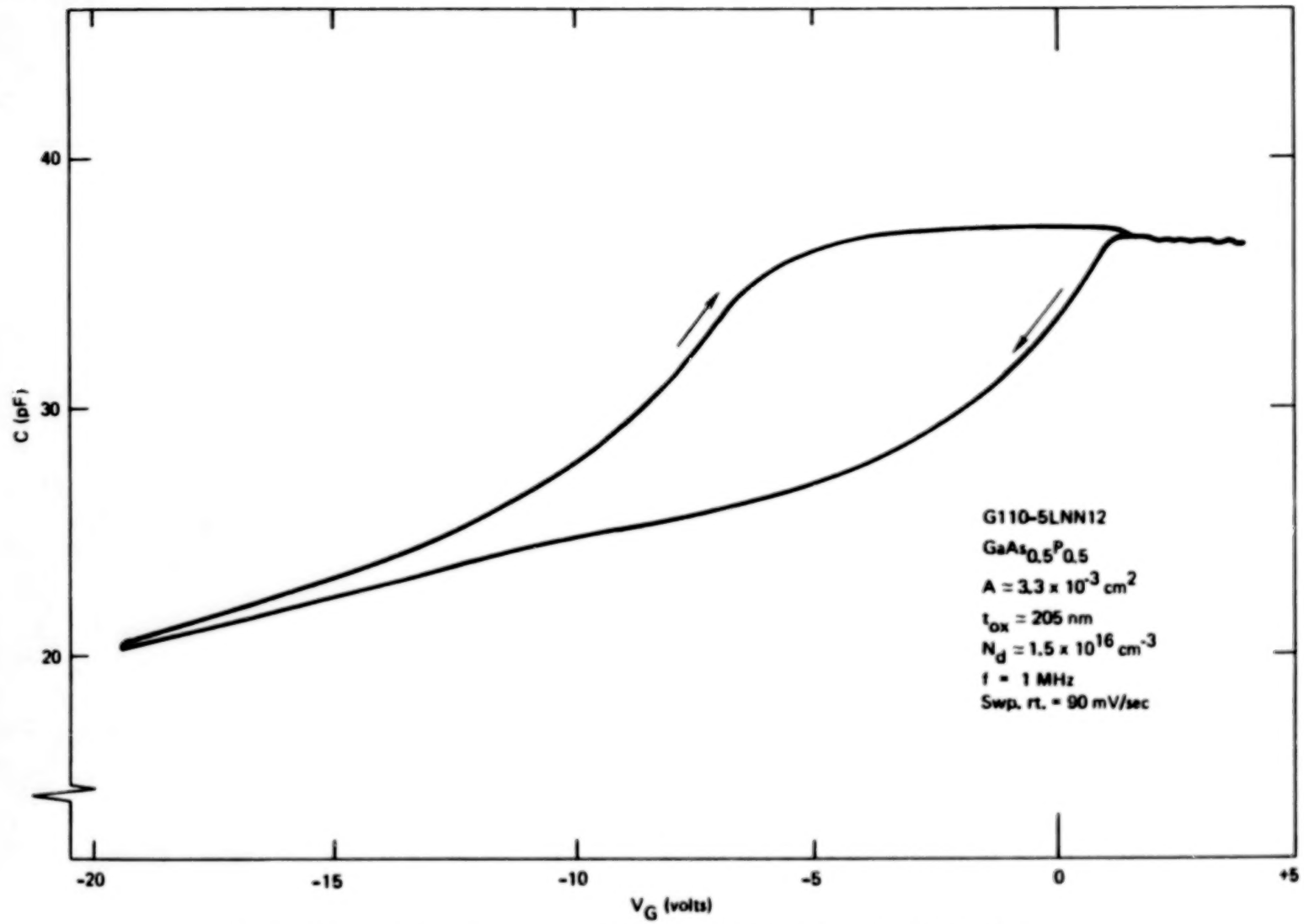


Figure 8(b). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristics for Dry Oxides Grown at 680°C, N_2 Anneal, 30 Min., 450°C

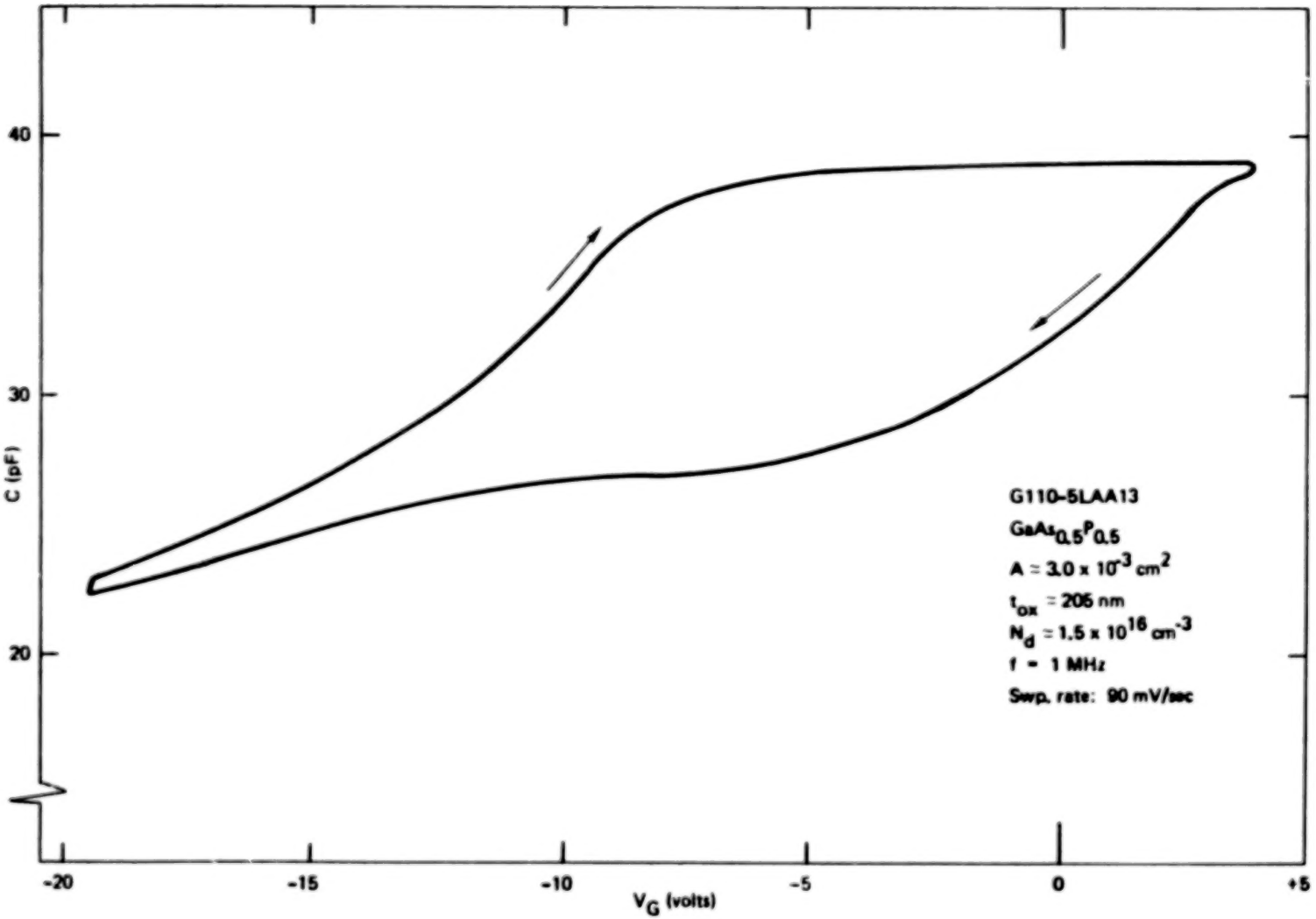


Figure 8(c). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristics for Dry Oxides Grown at 680°C, Ar-Anneal, 30 Min., 450°C

In an attempt to examine the effects of a lower temperature oxidation on interface characteristics, some films were grown at 600°C in steam at atmospheric pressure. Figure 9 shows the C-V characteristics of a device with an insulator which was grown for 225 minutes in steam at 600°C. This growth was followed by a drying out process in dry O_2 at 600°C for 2 hours, and then in argon at 600°C for 30 minutes. The magnitude of hysteresis is somewhat larger than that for the dry oxides in Figures 4, 5 and 6, but the equivalent transferred charge density ($N_t = C_i \Delta V_{FB}/qA$) remains about 1.2×10^{12} cm^{-2}.

As will be discussed in the next section, ion microprobe analyses indicate a loss of arsenic from the surface of the oxide following argon annealing. This arsenic may be in the form of As_2O_3 which was outdiffusing during the growth process. (As_2O_3 vapor press. = 1 atm. @ 457°C.) The lower temperature anneal would not be expected to result in as much arsenic loss as occurs at 680°C. No significant changes in the arsenic profile near the oxide-semiconductor interface is observed with the IMMA. It is in this region that any changes in composition are expected to result in measurable changes in trapping behavior and C-V hysteresis. It is possible that a crystallization or phase transition of arsenic or phosphorus or one of their compounds may be occurring at this interface causing changes in trapping behavior.

Accumulation Capacitance and Dielectric Constant Anomalies -- The C-V characteristics shown in Figures 4 and 5 exhibit various inconsistent and anomalous aspects with regard to accumulation capacitance values. All of the devices represented by the curves had dielectrics which were grown during the same oxidation run. For a more direct comparison, Figure 10 is a C-V characteristic of an Ar-annealed $GaAs_{0.5}P_{0.5}$ MIS device also fabricated during the same run but which had a higher starting material donor concentration ($\sim 9 \times 10^{16}$ cm^{-3}). Comparison of this curve with that of Figure 5(b) indicates a difference in the nature of the hysteresis and widely differing "accumulation" capacitance values per unit area. Table II summarizes the accumulation capacitance and "dielectric constant" values obtained from the C-V characteristics of Figures 4, 5 and 9. The dielectric constant values determined for the more heavily doped material agree with values obtained previously (Reference 3) and is in the range reported for many dielectrics grown on GaAs and GaP (Reference 7 and 8)

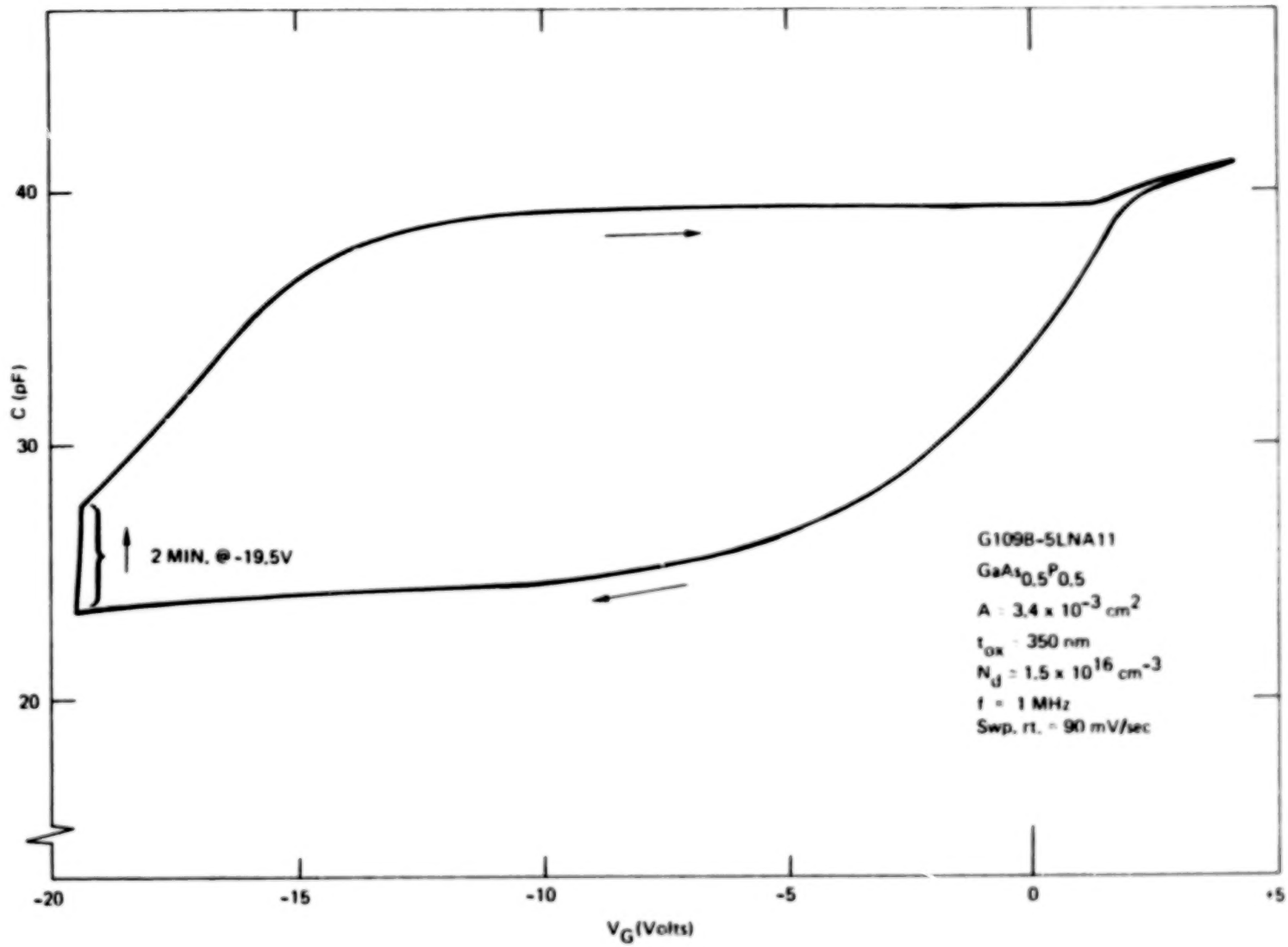


Figure 9. $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristic for Steam Oxide Grown at 600°C

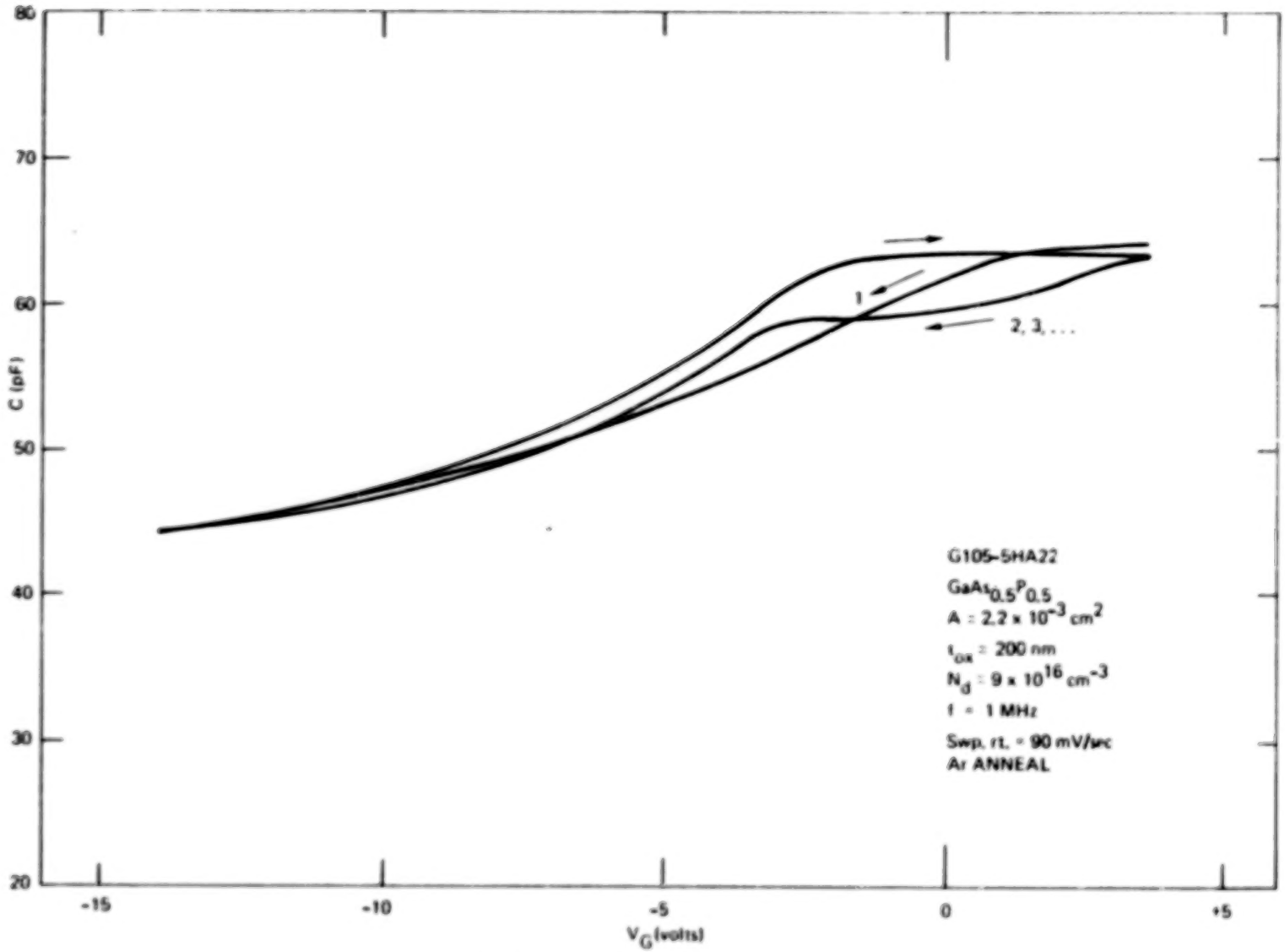


Figure 10. MIS C-V Characteristic Annealed Dry Oxide Grown on Heavily-Doped $GaAs_{0.5}P_{0.5}$

Table II. Comparison of Accumulation Capacitance and Dielectric Constants Deduced from C-V Characteristics for Dry Oxidation

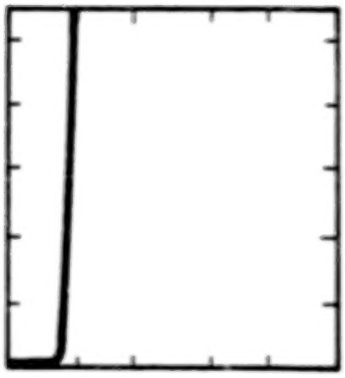
Device No.	Substrate	$N_d(cm^{-3})$	Anneal	$t_{ox}(\mu m)$	$C_i/A(F/cm^2)$	ϵ_r
4N15	$GaAs_{0.6}P_{0.4}$	7×10^{16}	No	230	2.5×10^{-8}	6.50
4A12	$GaAs_{0.6}P_{0.4}$	7×10^{16}	Argon	230	2.65×10^{-8}	6.89
5HA22	$GaAs_{0.5}P_{0.5}$	9×10^{16}	Argon	200	2.86×10^{-8}	6.46
5N15	$GaAs_{0.5}P_{0.5}$	1.5×10^{16}	No	200	1.79×10^{-8}	4.04
5A22A	$GaAs_{0.5}P_{0.5}$	1.5×10^{16}	Argon	200	1.01×10^{-8}	2.29

with similar impurity levels. The more lightly doped semiconductor, however, yields dielectric constants that are only about 60 percent of those for the more heavily doped material in the unannealed case, and about 35 percent for the annealed case.

The anomalous ε_r values for lightly doped $GaAs_{0.5}P_{0.5}$ were investigated further by examining the C-V and I-V of the Schottky diodes used for determining impurity levels in the epitaxial layers. Figure 11 shows Schottky current-voltage characteristics for the n-type $GaAs_{0.5}P_{0.5}$ diodes. The forward and reverse characteristics for the lightly doped material both indicate reverse-biased diode behavior. In addition, the capacitance of the lightly doped diodes saturated at a value of 2.73×10^{-8} F/cm^2 in the positive (forward) bias portion of the C-V characteristic. This behavior suggests the presence of a fixed capacitance in series with the diode. When this capacitance is subtracted from the measured accumulation capacitance of Device No. 5N15 in Table II, a dielectric constant of 11.77 is calculated, much higher than that for the heavily doped devices. It is apparent that there is no simple explanation for these results.

Anomalous intrinsic or p- layers have been previously observed between n^- GaAs epitaxial layers grown on n^+ GaAs substrates (Reference 11), and were attributed to autodoping of an amphoteric impurity such as silicon during growth, or to stress-induced changes. It is possible that either or both of these phenomena may be responsible for the present results.

The decrease in the C_i/A value for lighter doped $GaAs_{0.5}P_{0.5}$ devices undergoing post-oxidation annealing is not understood. No change in oxide thickness is noted following annealing. In many cases, annealing anodic oxides on GaAs about 450°C results in arsenic loss and densification of the film, which would tend to increase the insulator capacitance (assuming no significant change in ε_r as arsenic is lost). This cannot explain the present case [Figures 5(a) and (b)] for $GaAs_{0.5}P_{0.5}$, where C_i decreases after annealing. It is possible that a change in the dielectric constant could occur with the loss of arsenic, but is not expected to be as significant as shown in Table II. It is apparent that this phenomenon requires further investigation before more definitive answers can be given.

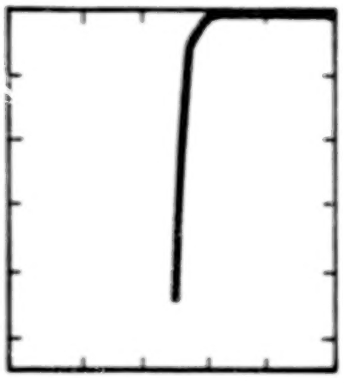


(a)

VERT: 100μA/DIV
HORIZ: 2V/DIV

$N_d \approx 9 \times 10^{16}$ cm^{-3}

Forward Characteristic



(b)

VERT: 100μA/DIV
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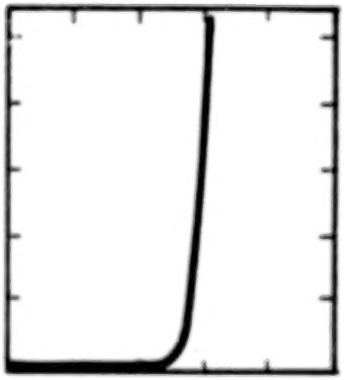
$N_d \approx 9 \times 10^{16}$ cm^{-3}

Reverse Characteristic



(c)

VERT: 100μA/DIV
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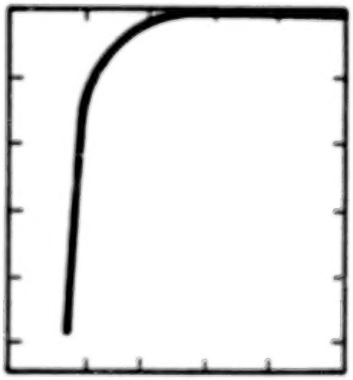
$N_d \approx 1.5 \times 10^{16}$ cm^{-3}

Forward Characteristic



(d)

VERT: 100μA/DIV
HORIZ: 10V/DIV

$N_d \approx 1.6 \times 10^{16}$ cm^{-3}

Reverse Characteristic

Figure 11. Forward and Reverse I-V Characteristics of Al-$GaAs_{0.5}P_{0.5}$ Schottky Diodes

Interface State Density Determination -- Attempting to determine the "fast" interface state density in $GaAs_{1-x}P_x$ MIS devices which exhibit hysteretic deep depletion C-V characteristics of the type described above presents many difficulties. Traditional analyses used for SiO_2-Si MOS devices, such as differential capacitance, quasi-static, and ac conductance, each may possess severe limitations or total inapplicability when applied to these widegap MIS structures.

A previous analysis of $GaAs_{0.5}P_{0.5}$ MIS structures using the ac conductance technique yielded ambiguous results (Reference 3), as it has previously with GaAs MIS devices (Reference 12). The quasi-static C-V method is probably also inapplicable to these devices because of the requirement for very low insulator leakage current and the existence of thermal equilibrium conditions in the semiconductor. Such is not the case for the present devices, where equilibrium conditions apparently do not exist due to low generation rates and/or moderate dielectric leakage.

The differential C-V (Terman, Reference 13) method is the most commonly used technique for analyzing III-V compound semiconductor MIS devices at the present time. Because of the moderate-to-high interface state values usually measured ($\geq 5 \times 10^{11}$ cm^{-2} eV^{-1}) for these devices the Terman method appears to provide adequate accuracy for analysis. In the present case, however, there is the additional complication of injection-type hysteresis, due to slow oxide traps, which can affect the determination of the "fast" state density. With this limitation in mind, however, the Terman method can provide a basis for comparing the properties of compound semiconductor-oxide interfaces as new analysis methods and knowledge develops. This method was applied to the $GaAs_{1-x}P_x$ MIS C-V characteristics (positive-going sweep) using ideal curves generated neglecting the contribution of minority carriers. This approach results in "state" values of 5-9 x 10^{11} cm^{-2} eV^{-1} for unannealed $GaAs_{0.5}P_{0.5}$ devices and 1-3 x 10^{12} cm^{-2} eV^{-1} for unannealed $GaAs_{0.6}P_{0.4}$ devices.

The comparison between the ideal characteristic and the initial negative-going sweep of the annealed $GaAs_{0.6}P_{0.4}$ device of Figure 4(b) is shown in Figure 12(a). The fit is very good in the accumulation region in this case. Analysis of the depletion portion of the characteristic results in "state" values of 1.7 x 10^{11} cm^{-2}-eV^{-1}, uniformly distributed in energy.

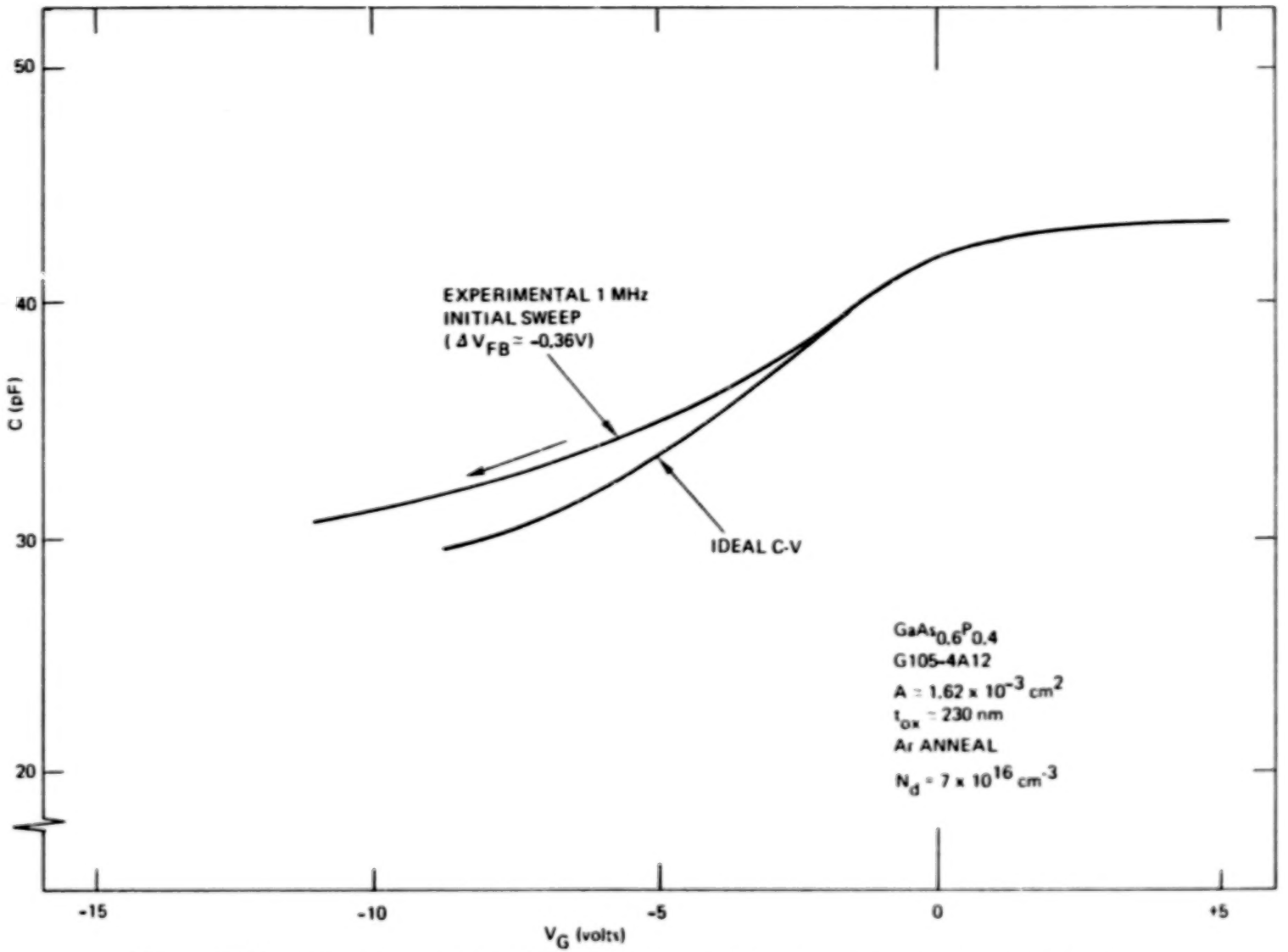


Figure 12(a). Comparison of Ideal and Experimental C-V Characteristics of $GaAs_{0.6}P_{0.4}$ MIS Device:Initial Negative Sweep

The experimental C-V characteristics of several annealed and lightly-doped devices could not be fitted in the accumulation regime to ideal curves of various doping levels. Figure 12(b) shows a comparison of the positive-going sweep of Figure 4(b) with the ideal characteristic. The increased slope ($\Delta C/\Delta V$) of the experimental curve in the region of the curve near accumulation could be resulting from dielectric leakage current which causes a departure from the ideal assumption of no leakage. Another possible reason for this type of characteristic is that the semiconductor surface potential is being "pinned", resulting in the somewhat lower constant capacitance with gate voltage. [It is noteworthy that the initial negative sweep can be repeated after the device is illuminated or undergoes B-T stressing (see Section V)].

If the characteristic of Figure 12(b) is analyzed in the depletion regime a uniform state density of 1.7×10^{11} cm^{-2}-eV^{-1} again results. It should be pointed out that these values are in the range where the Terman analysis begins to result in limitations in accuracy.

The major precautions that should be taken when attempting to interpret the results presented above is that the term "fast" interface state in the Si-SiO_2 technology probably cannot be analogously applied to III-V structures which have significant slow oxide-trapping effects. With this in mind, the C-V analysis appears to be useful in providing a semiquantitative comparison of the effects of annealing on interface characteristics. It is apparent that much additional effort is needed to provide adequate quantitative interface analysis techniques for widegap MIS devices.

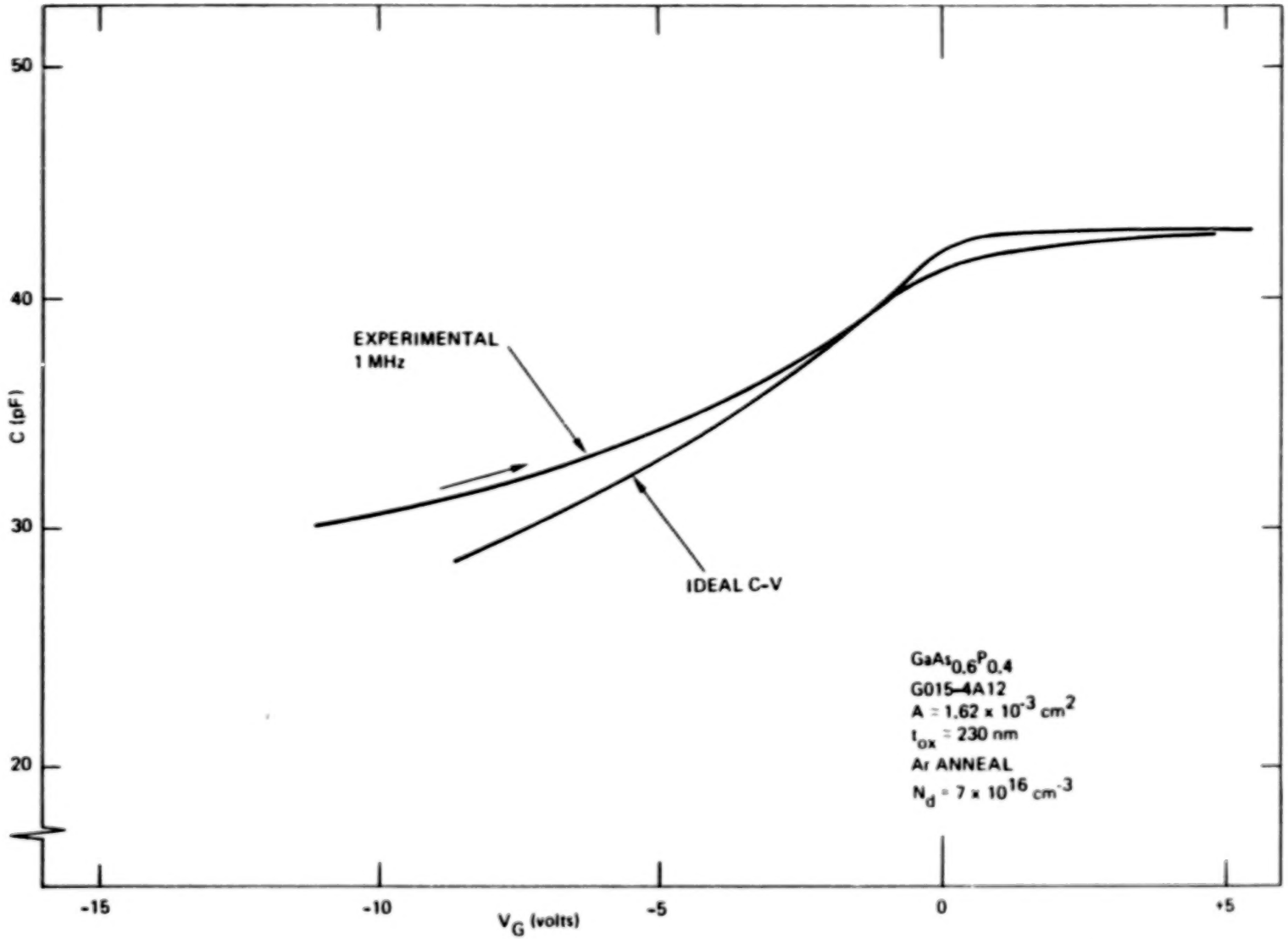


Figure 12(b). Comparison of Ideal and Experimental C-V Characteristics of $GaAs_{0.6}P_{0.4}$ MIS Device:Positive Sweep

SECTION IV

SECONDARY-ION MASS SPECTROMETRY TO DETERMINE DIELECTRIC COMPOSITION AND STABILITY

The use of secondary ion mass spectrometry to determine the elemental composition of the dielectric is described in this section. A discussion of the various features and limitations of this technique is given, followed by experimental depth profiles of $GaAs_{1-x}P_x$ MIS structures. The chemical stability of the structures after various bias-temperature stress treatments will be discussed in the following section.

Secondary Ion Mass Spectrometry

In the Secondary Ion Mass Spectrometry (SIMS) technique (Reference 14), a beam of energetic (1-20 keV) ions bombards the sample. The interaction of these ions with the solid results in the ejection of substrate atoms and molecules in both neutral and charged states from the first few monolayers [typically <2 nm (20 Å)]. The charged particles sputtered from this surface region are then mass and charge analyzed and finally detected. Through high sensitivity mass spectrometric techniques, SIMS has achieved much higher detection sensitivities than all other surface analytical techniques, with detection limits $<10^{17}$ atoms/cm^3 possible for many different element/matrix combinations. In addition, depth concentration profiling of trace constituents with depth resolutions <50 Å has also added to the interest in SIMS.

Several models utilizing various physical mechanisms have been proposed to explain the general trends of secondary ion emission. While these models have enjoyed varying degrees of success, there is, at present, no single theoretical treatment to accurately predict the ionization probability of an element in any matrix. Therefore, quantitative or semi-quantitative SIMS has relied on the analysis of standards which have been characterized by other analytical methods. Even when basing quantitation of an unknown sample on results obtained on standards, there are other limiting aspects. These limitations are discussed below.

Limitations to Quantitative SIMS

The effects limiting quantitative SIMS analysis can generally be classed as follows: (1) secondary ion yield differences, (2) masking of secondary ion species by undesired ionic species, and (3) incident ion effects. These effects are discussed briefly in the following paragraphs.

Secondary Ion Yield Effects -- The major factors influencing ion yield are the electronic and chemical properties of the sample surface, which are due to the basic characteristics of the matrix, and the equilibrium concentration of absorbed active species (including implanted primary ion beam species). The ratio of the secondary ion yield of a given element relative to that of another element present in the same matrix can exceed 10^4. In general, however, this spread in relative yield decreases as the matrix changes from a metallic character to an oxide or insulator. The use of a reactive primary ion beam (particularly oxygen) can also alter the characteristics of the matrix to enhance ion yields. These secondary ion yield differences are more important than ion sputtering rate differences between the different matrix elements. Sputtering rates typically differ by less than a factor of ten, and this difference decreases with increasing primary beam energy.

Secondary Ion Species Interferences -- Because SIMS detection is basically a measurement of the mass to charge ratio, and because there are several different molecular ionic species which may possibly have the same mass/charge ratio as the element or molecule of interest, it is possible to sometimes obtain erroneous results through mass interference. Fortunately, the abundance of molecular species falls off rapidly as the number of particles in combination increases. Also, some idea of the sample composition is generally known, prior to SIMS analysis, so that possible interferences can be inferred, before a detailed analysis is carried out.

Incident Ion Effects -- Several characteristics of the incident ion beam can directly or indirectly influence secondary ion emission. These characteristics include beam energy, mass and angle of incidence, primary ion current density, and the chemical nature of the incident ions.

The energy, mass, and angle of incidence control the collision cascade in the surface layer of the solid sample. The principle energy effect is on ion yield. In general, higher beam energies result in greater ion yield. For energies above a few keV, this effect saturates and yield is constant for increasing energy. In addition to yield effects, the beam energy will also determine subsurface layer mixing and matrix effects and the depth of the incident ion implant zone. Subsurface mixing and matrix effects are important in depth profiling where a significant ion dose is deposited in order to achieve a relatively high sputtering rate. If a chemically reactive beam such

as oxygen is used this high implanted dose (> 10^{15} ions/cm^2) can alter the matrix and enhance positive ion yield. The depth (energy) of the implanted ions will then determine when this enhancement effect stabilizes. Stabilization generally occurs at a depth of $R_p + 2\Delta R_p$, where R_p is the projected ion mean range and ΔR_p is the standard deviation of the mean range. This effect will be discussed later in relation to the present study.

In addition to effects related to chemical interaction of the primary beam with the substrate matrix, differential "knock-in" effects can occur for sufficiently high beam energy and mass. Because of differences in cross sections certain atoms can be knocked deeper into the substrate than others. "Knock-in" effects can play an important role in interface profiling. The "knock-in" effect is, in general, more prevalent for higher incident beam energies and masses.

Quantitative analysis using SIMS has generally not been successful because of the limitations discussed above. However, the technique is attractive for qualitative analysis and for observation of relative changes in the composition of solids, as in the present study.

Ion Microprobe Mass Analysis

Ion Microprobe Mass Analysis (IMMA) is basically the same as secondary ion mass spectrometry. The ion microprobe utilizes a smaller diameter primary ion beam of higher energy than generally used in most SIMS instruments. These features allow the capability for rapid measurement of depth profiles in microarea regions of the sample of interest.

The instrument used in the present investigation* is schematically illustrated in Figure 13. The ions used to bombard the sample are generated in a hollow cathode duoplasmatron ion source which is capable of producing ions of a variety of different gases. The primary magnet is used to mass separate the primary ion beam to ensure that only a single ion species bombards the sample. A set of electrostatic deflection plates just below the magnet guide the beam through apertures to electrostatic condenser lenses. These lenses successively demagnify and focus the beam to spot sizes ranging from 2 to 500 μm in diameter.

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*ARL Ion Microprobe Mass Analyzer, operated by the Aerospace Corp., El Segundo, California.

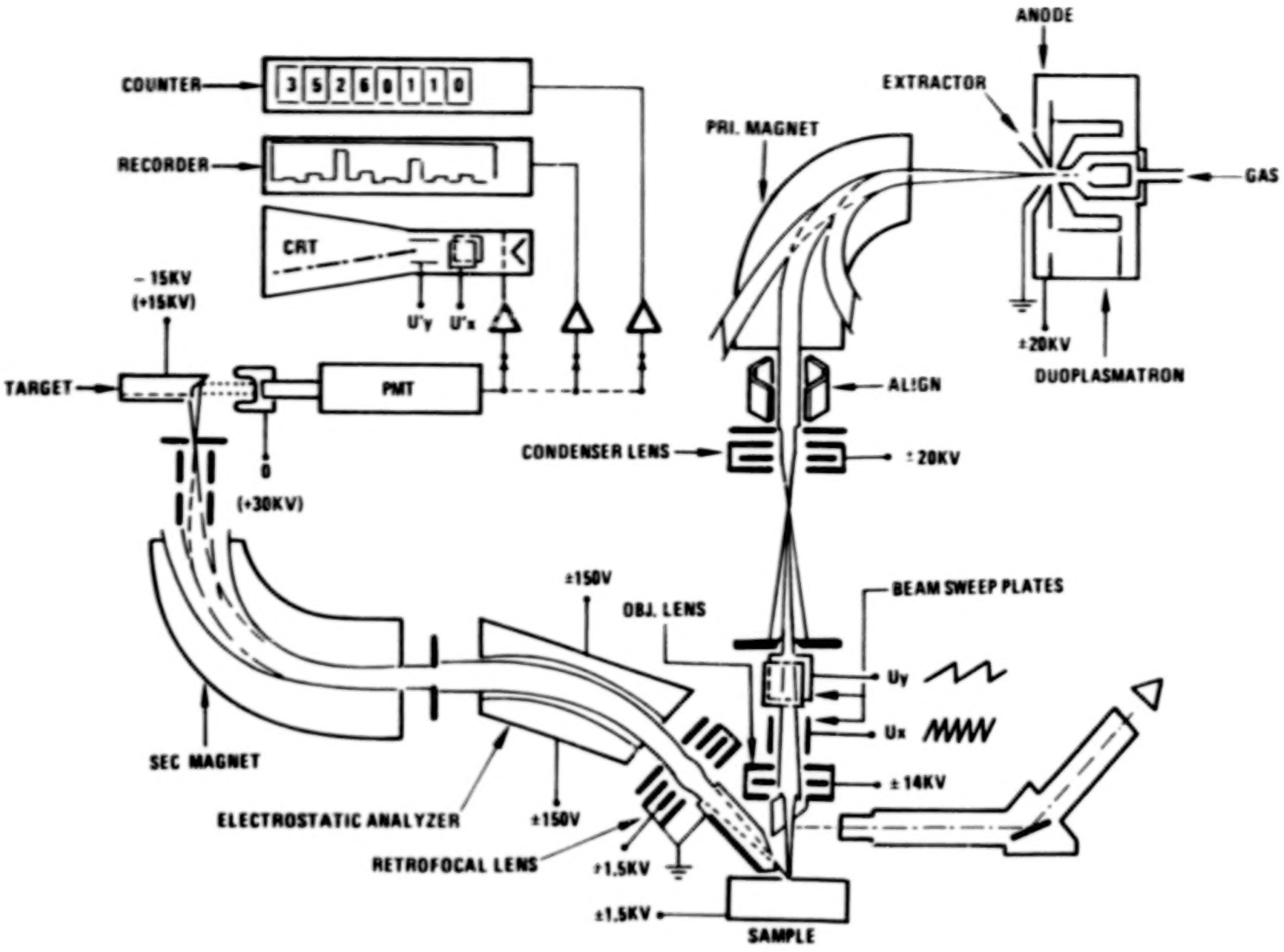


Figure 13. Ion Microprobe Mass Analyzer (IMMA)

After bombardment of the sample, the sputtered ions are collected and analyzed in a double-focusing magnetic mass spectrometer. The mass-analyzed ion beams are detected with a high-gain Daly-type device which permits single counting of both positive and negative ions. The resolved ion signals can be read as count rates or as direct currents on a chart recorder.

In addition to fixed point bombardment the incident ion beam can be swept in a raster over a selected area of the sample using sweeping plates in the primary lens column. By synchronization of the beam sweep with the sweep of a CRT display a direct ion intensity image of the analyzed area can be viewed.

One of the major advantages of the IMMA over conventional SIMS is its use of electronic aperturing to eliminate crater wall effects during depth profiling. These effects are shown in Figure 14. In a stationary focused ion beam, the ion current density incident on the sample is not constant over the beam diameter, resulting in nonuniform layer removal. If the detection area for secondary ions exceeds the total beam area, contributing ions from the crater edges will distort the profile. To eliminate this effect, the focused ion beam is electronically swept over an area large enough to provide a uniform current density in the central region. The secondary ion detection system is then gated to accept ions only when the primary beam is within this selected window of uniform current density. In the instrument used for this study, the central window area comprised about 16 percent of the total raster area.

Ion Beam Species, Energy and Primary Ion Beam Current

For the experiments reported here, the primary ion beam used was $^{16}O_2^+$. The anode potential was 20 kV and the sample potential was maintained at 1.5 kV. Subtracting the sample bias from the primary accelerating bias, and dividing the energy between the two oxygen atoms results in an equivalent energy of 9.25 keV for each $^{18}O^+$ ion. As mentioned previously, use of a reactive beam results in higher positive secondary ion yields. This particular oxygen isotope (i.e., $^{18}O^+$) was used because of the interest in determining the oxygen profile in the dielectric region of the MIS structures. The use of $^{16}O^+$ or $^{32}O_2^+$ as a primary beam would result in interference effects during the detection of $^{16}O^+$ secondary ions from the sample.

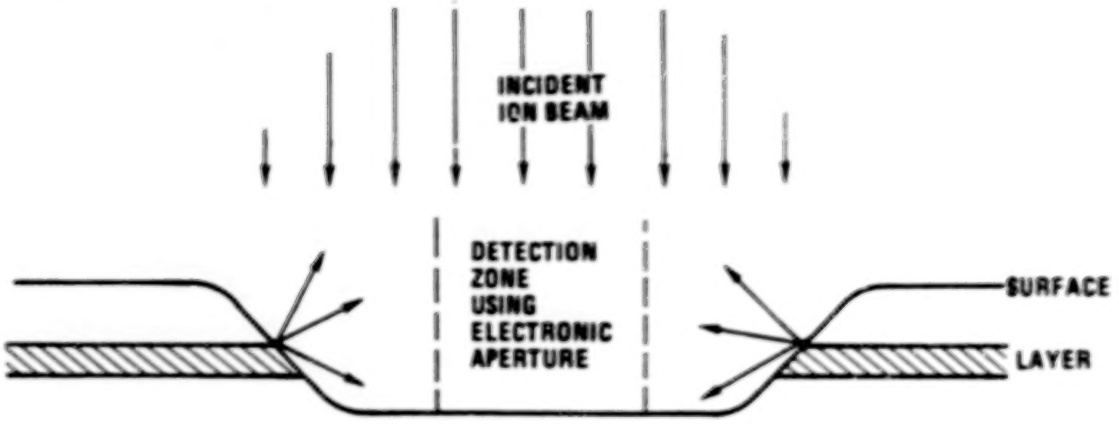


Figure 14. Illustration of Cratering Effects and Use of Electronic Aperturing

The primary ion beam currents used for the IMMA are typically 10 nA for depth profiling and 1 nA for surface analysis and ion image displays. For the particular matrices (thin film insulators and semiconductors), beam energy, and analysis areas used here, these current densities result in sputtering rates of the order of 0.17 nm/sec (~100 Å/min.) for profiling and 0.02 nm/sec (~10 Å/min.) for surface scans.

Compositional Analysis of Oxides Grown on $GaAs_{1-x}P_x$

Dry Oxide Composition -- Figure 15 is an ion microprobe depth profile of the secondary ion count rate versus sputtering time for an oxide grown on $GaAs_{0.5}P_{0.5}$ in dry O_2 at 700°C for 370 minutes. This profile is uncorrected for sputter rate and ion yield differences between the elements; however, several general observations regarding the behavior of the phosphorus and arsenic during oxidation can be made.

The similarity between the phosphorus and oxygen profiles in the bulk of the oxide indicates the probability of a chemically bonded compound, such as $GaPO_4$. Other possible phosphorus compounds, such as P_2O_5, are not expected to be present in the film because of their volatility at the growth temperature. This rise in the phosphorus counts

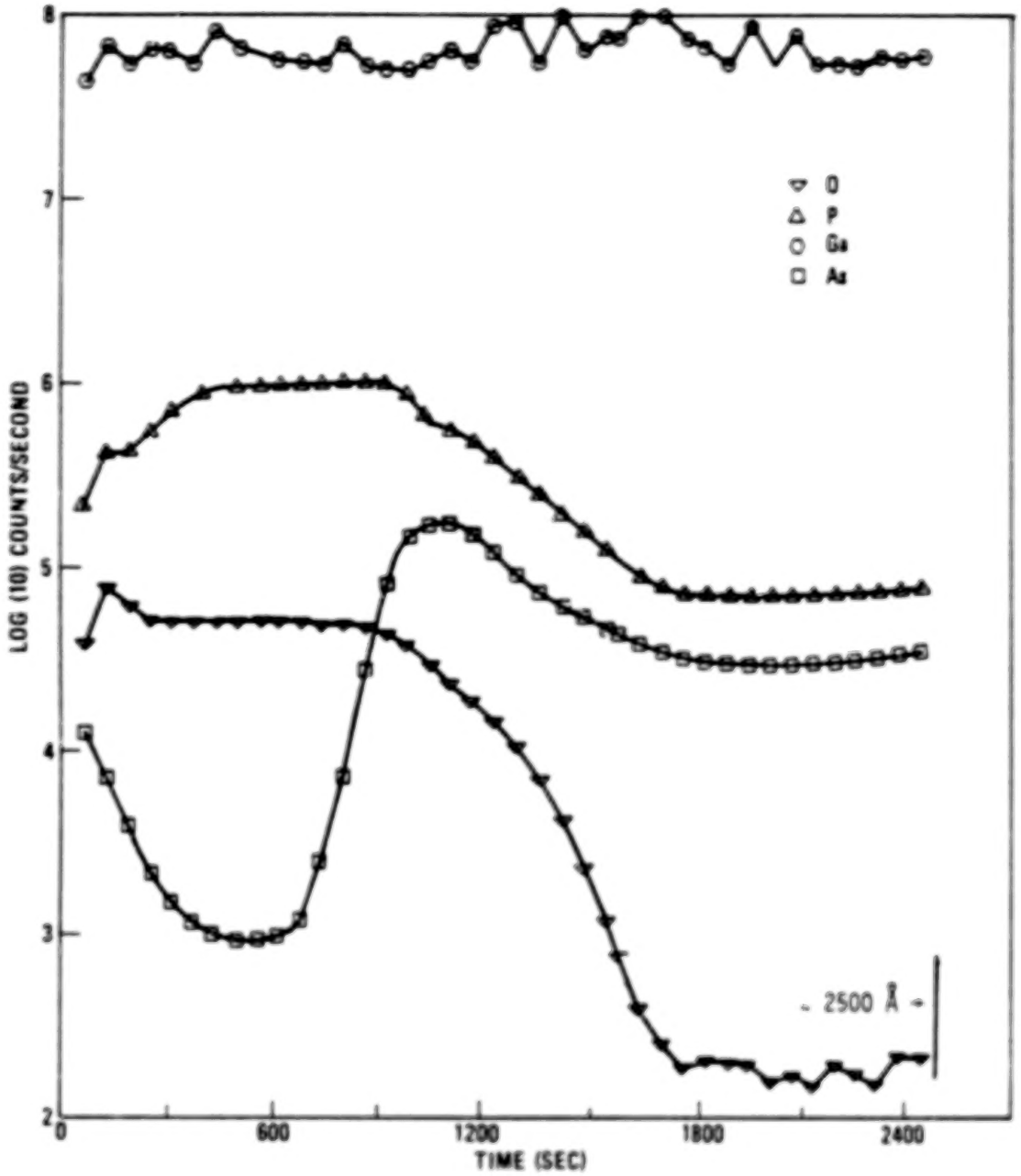


Figure 15. IMMA Profile of $GaAs_{0.5}P_{0.5}$ Dry Oxide

near the oxide surface may be due to the increase in ion yield due to the implanted $^{18}O^{+}$ ions, as discussed earlier. This effect is more clearly demonstrated in the IMMA profile of the $GaAs_{0.5}P_{0.5}$ starting material shown in Figure 16, where equilibrium of the sputtered ion yield is reached at about 200 sec. (~450 Å). This depth corresponds approximately to the value $[R_p + 2\Delta R_p]$, discussed earlier, for oxygen.

The behavior of arsenic in the oxide of Figure 15 is similar to that observed in oxides grown on GaAs. The rise in As counts near the surface of the oxide is similar to that noted with plasma-grown oxides on GaAs (Reference 15). The major portion of the oxide is arsenic-deficient, and there is apparently an arsenic-rich region near the oxide-semiconductor interface. It cannot be concluded simply from the raw count data that an arsenic-rich region is present because of possible matrix and sputtering yield effects. Obtaining more quantitative results requires the use of sample standards of similar composition to the unknown to obtain the appropriate sensitivity factors to be used for reduction of the raw count data.

A preliminary attempt was made to semi-quantify the data of Figure 15 using an internal standards method. In this method, counts of a standard sample of a "known" composition (in this case the $GaAs_{0.5}P_{0.5}$ starting material) are used to generate sensitivity factors which are then applied to the data from the unknown sample (oxidized $GaAs_{0.5}P_{0.5}$). Figure 17 shows the results when applied to the oxidized $GaAs_{0.5}P_{0.5}$ data of Figure 15. Unfortunately, the $GaAs_{0.5}P_{0.5}$ standard chosen in this case had a residual surface oxide layer which resulted in sensitivity factors which did not truly represent a pure $GaAs_{0.5}P_{0.5}$ matrix. The effect of this discrepancy is shown in the region of the profile corresponding to the bulk of semiconductor, where the gallium concentration is too high relative to the phosphorus and arsenic levels. The oxide-semiconductor interface region appears to be arsenic-rich in that the arsenic level is above the gallium level. As mentioned earlier, ion yields are matrix-dependent and applying sensitivity factors determined for the semiconductor to the oxide matrix, as was done here, may not result in precisely accurate concentration profiles. Therefore, it should be kept in mind that Figure 17 represents only a preliminary attempt at semi-quantifying IMMA data, and that further

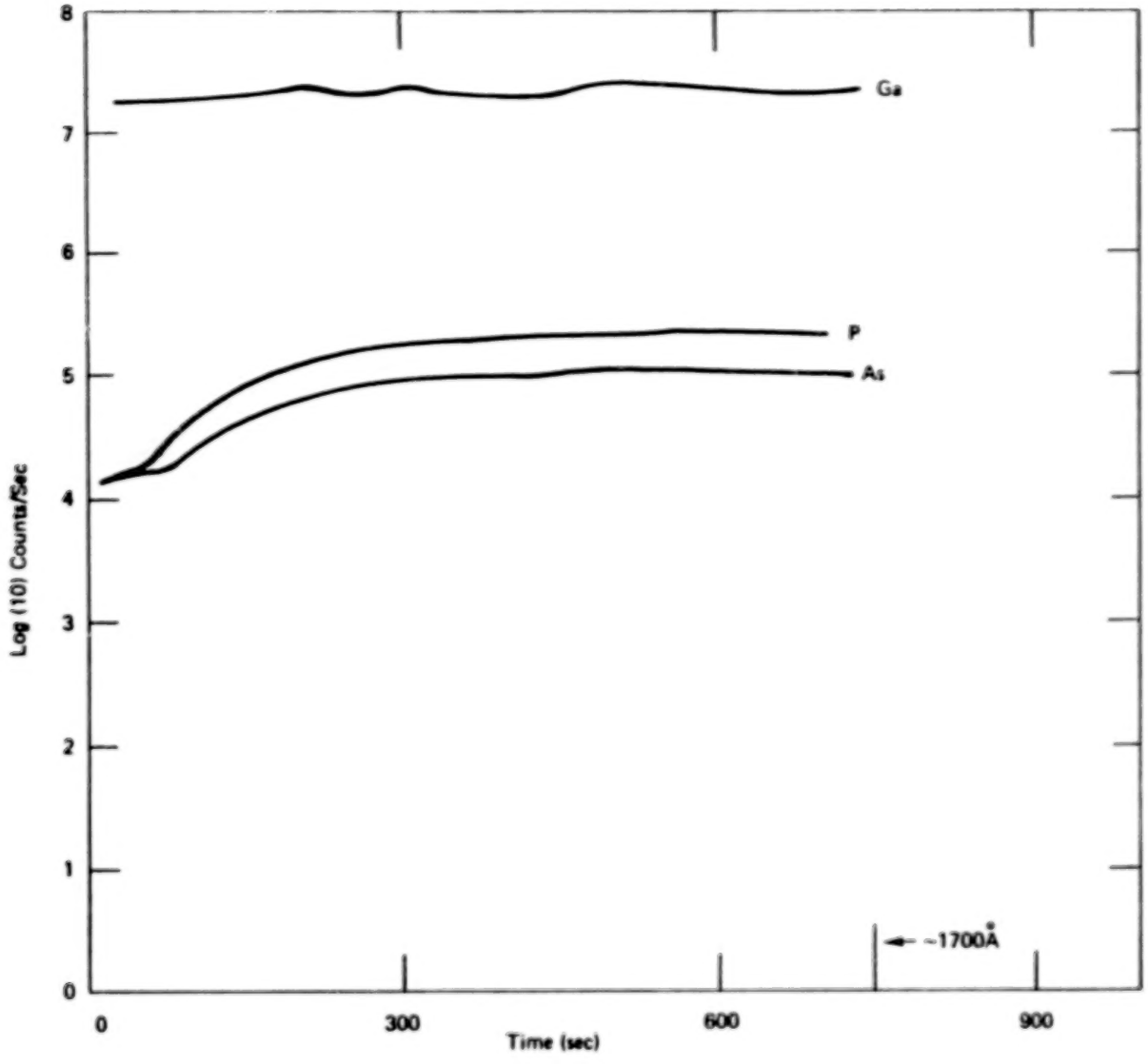


Figure 16. IMMA Depth Profile of $GaAs_{0.5}P_{0.5}$ Starting Material

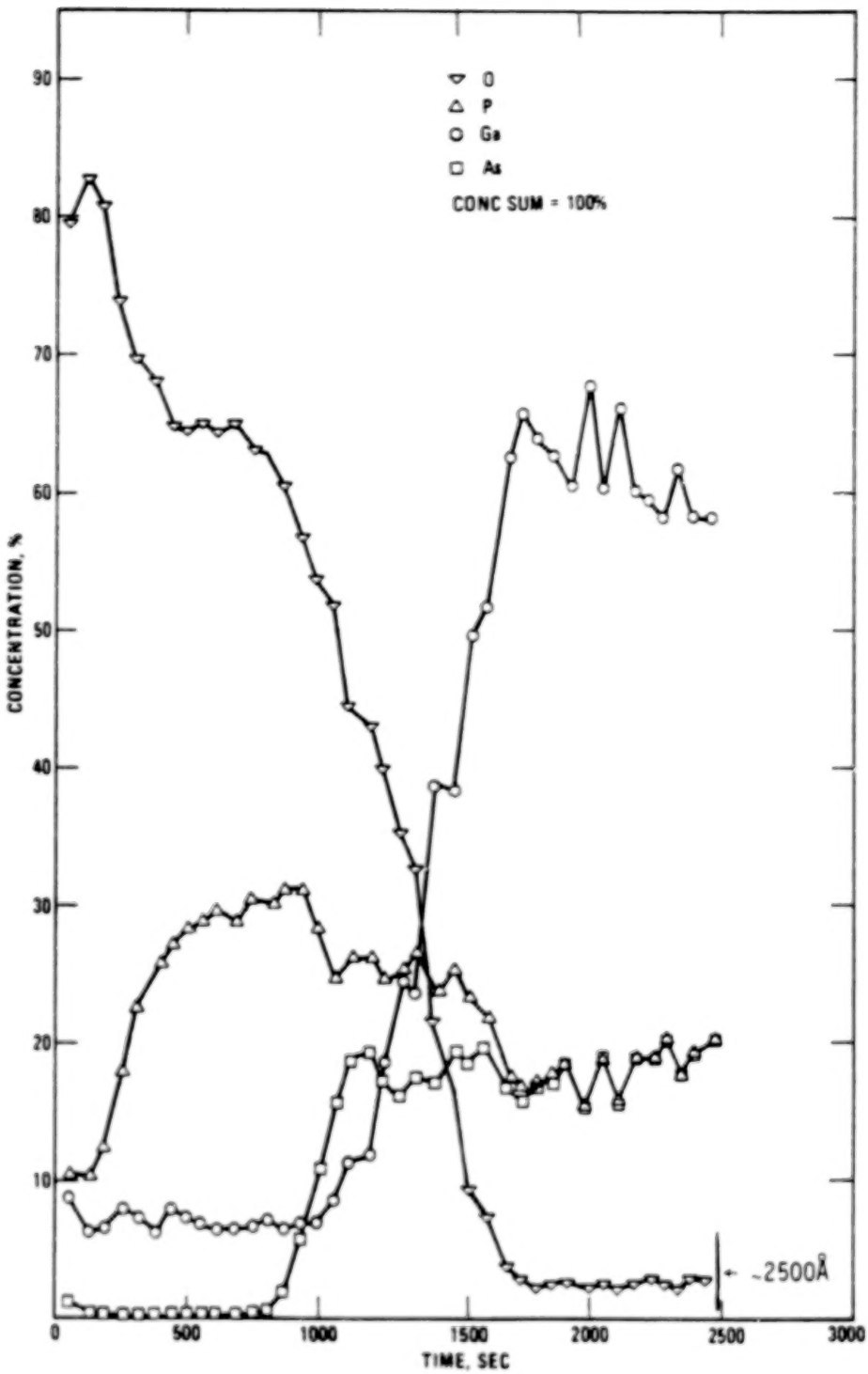


Figure 17. Composition Profile of $GaAs_{0.5}P_{0.5}$ Dry Oxide Using Sensitivity Factors from $GaAs_{0.5}P_{0.5}$ Starting Material

improvements in the analysis will be possible when the IMMA data can be correlated with that obtained by other methods, such as Auger and X-ray photoelectron spectroscopy.

Annealing Effects -- As discussed in the section on electrical characteristics, post-oxidation annealing generally results in a reduction of hysteresis in the capacitance-voltage characteristics and an increase in the dielectric leakage current. To examine if these effects are due to a change in the oxide elemental composition, IMMA profiles were obtained for annealed and unannealed samples. Figures 18(a) and (b) are $GaAs_{0.6}P_{0.4}$ profiles from the same wafers as the MIS capacitors whose C-V characteristics are shown in Figures 4(a) and (b). The general shape of the profiles are similar to each other and to the $GaAs_{0.5}P_{0.5}$ profile of Figure 15, However, comparison of the arsenic profiles in Figure 18 shows that a definite drop in the surface region peak occurs for the annealed oxide. The slight drop in the interface region peak is probably due to a slight decrease in the sputtering rate (avg. sputtering rates: 1 Å/sec and 1.13 Å/sec). Profiles of $GaAs_{0.6}P_{0.4}$ and $GaAs_{0.5}P_{0.5}$ MIS structures show similar surface arsenic loss (see the following section), without any changes in the interface arsenic peak.

The arsenic loss near the surface is probably due to the volatilization of arsenic oxide (As_2O_3 vapor press. = 1 atm. @ 457°C) which was outdiffusing during the growth process. This depletion is apparently related to the increase in leakage current and the decrease in hysteresis illustrated in Figure 4. However, it is expected that only major changes in composition or chemical bonding in the oxide-semiconductor interface region would result in measurable changes in trapping behavior and hysteresis. It is possible that other analytical techniques, such as x-ray photoelectron spectroscopy (XPS) may be able to detect changes in bonding structure which may be resulting in changes in trapping characteristics.

Steam Oxide Composition -- As discussed earlier, methods were investigated for obtaining lower temperature oxides to examine the effect on both the electrical characteristics of MIS devices and the insulator composition. Figure 19 shows the IMMA profile of the same oxide whose MIS C-V characteristic is shown in Figure 9. The oxide was grown in steam at 600°C for 225

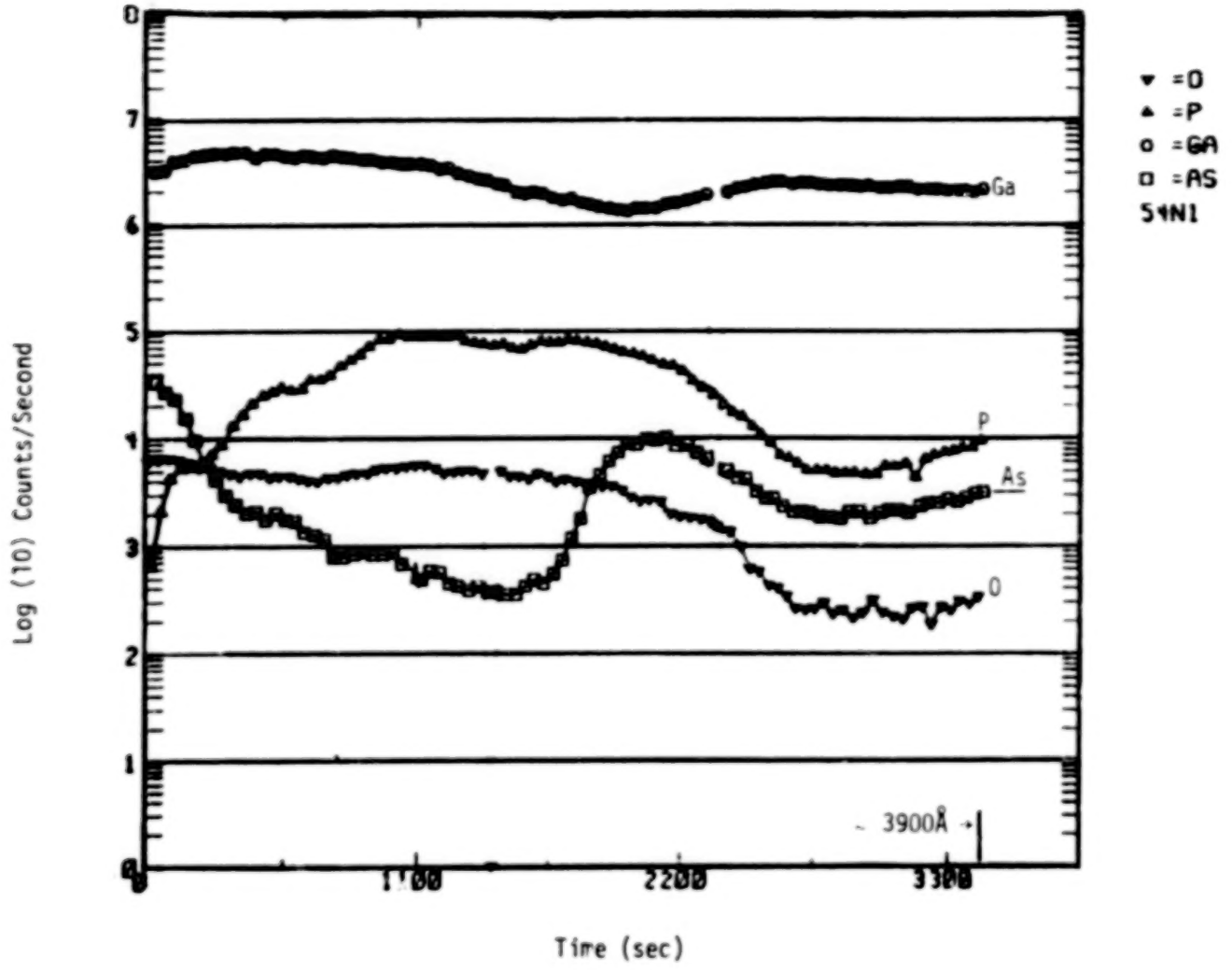


Figure 18(a). IMMA Profile of $GaAs_{0.6}P_{0.4}$ Dry Oxide--Unannealed

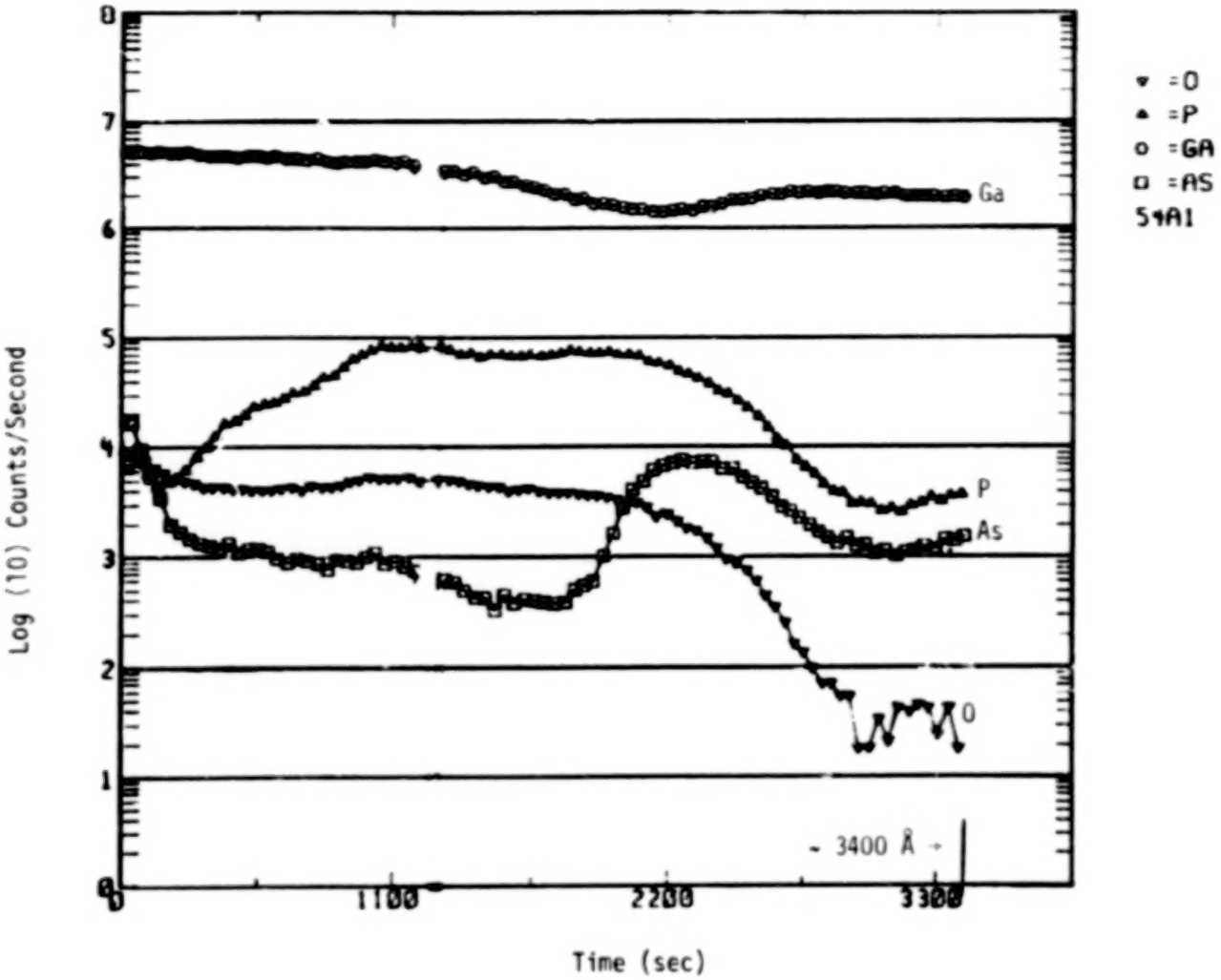


Figure 18(b). IMMA Profile of $GaAs_{0.6}P_{0.4}$ Dry Oxide--Ar-Annealed

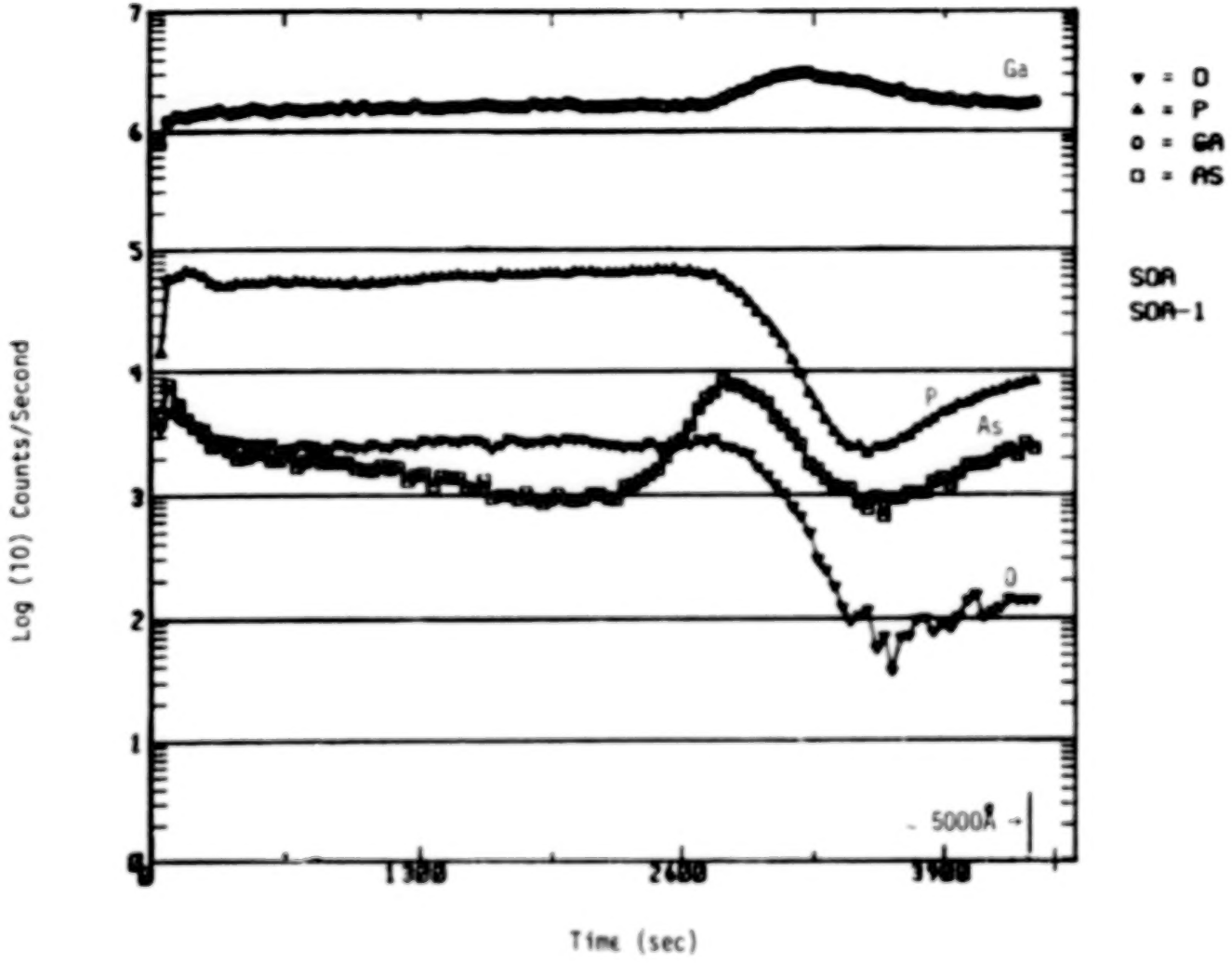


Figure 19. IMMA Profile of $GaAs_{0.5}P_{0.5}$ Steam Oxide

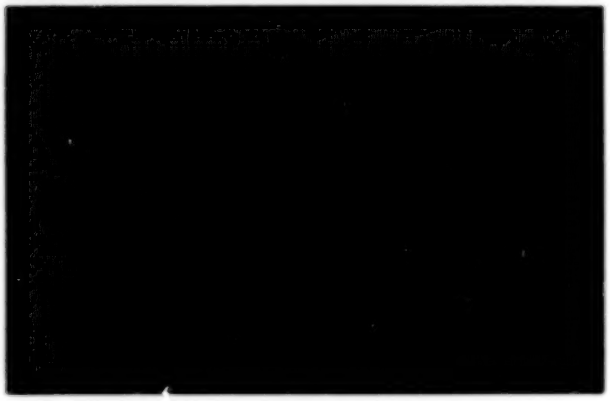
minutes, and was followed by a drying process in O_2 for 2 hours at 600°C and argon anneal at 600°C for 30 minutes.

The same general features exist in the IMMA profile of both the steam and dry oxides; however, the phosphorus and oxygen profiles appear to be more uniformly distributed through the bulk of the oxide grown in steam. No change was noted in either the C-V characteristics or the IMMA profile for an unannealed steam oxide grown at the same time as that in Figure 19.

Visual examination indicates that the surfaces of the 600°C steam oxides are somewhat less heterogeneous and structured than those of the higher temperature dry oxides. Reflection electron diffraction patterns tend to confirm this by showing only a faint non-oriented polycrystalline pattern, as shown in Figure 20.

It was observed during the etching of the steam oxide step used for thickness measurements that the residual layer left after etching in NH_4OH (see Section II) contained crystal-like areas, as shown in Figure 21(a). Figures 21(b) through (f) are ion micrographs for the various elements expected to be present. Only the phosphorus counts appear to show significant intensity at regions corresponding to the crystallites. These results are somewhat ambiguous, however, because the $^{18}O^+$ (probe ion) scan shows darker regions corresponding to the crystallites. This result indicates a difference in matrix effects of the "crystallites" from the field of the residual layer, possibly due to their vertical structure, which could cause varying ion yields. Without geometric and matrix effects the probe ion scan should be uniform.

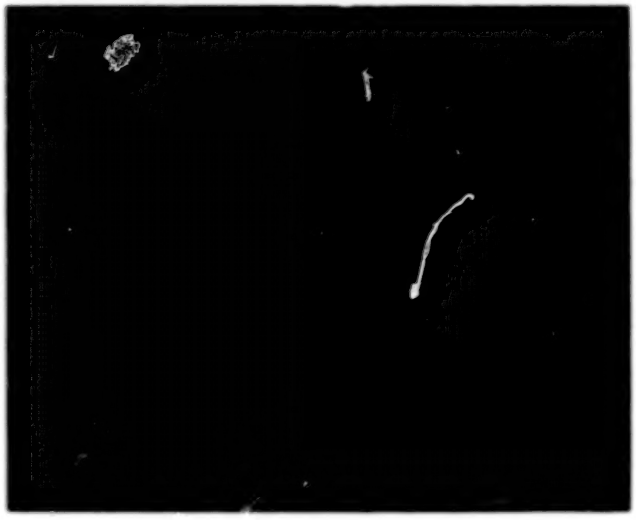
The uniformity of the arsenic scan indicates that the crystal-shaped regions are not crystalline As, as might be expected based on previous studies of thermal oxides grown on GaAs (Reference 16). The high $^{31}P^+$ intensity shown in Figure 21(d) cannot be correlated with increased $^{16}O^+$ counts. A strong correlation might have indicated the presence of $GaPO_4$ crystallites at the interface. Such a result would not be unexpected, because a metastable phase inversion of $GaPO_4$ occurs at 616°C (Reference 17). This phase inversion probability coupled with the fact that no large crystallite structure was observed in the interface region of the dry oxides suggest that different crystalline phases may exist in the steam and dry oxides. Therefore, further studies of this interesting phenomenon and lower temperature steam oxidation processes, in general, are indicated.



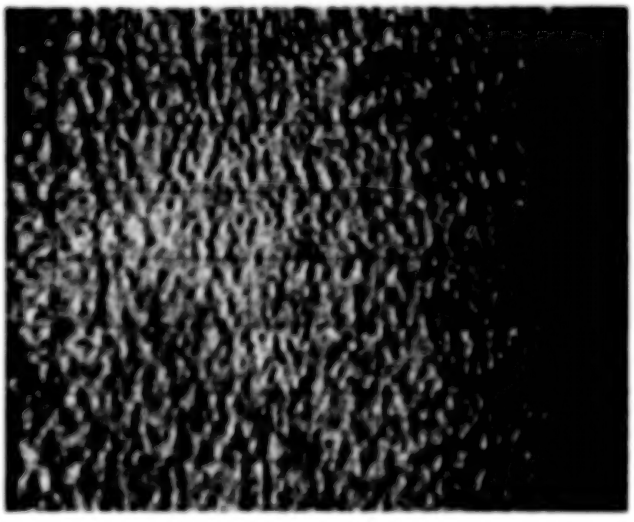
(a) Dry Oxide Grown at 680°C

(b) Steam Oxide Grown at 600°C

Figure 20. Reflection Electron Diffraction Patterns of Oxidized $GaAs_{0.5}P_{0.5}$ Surface



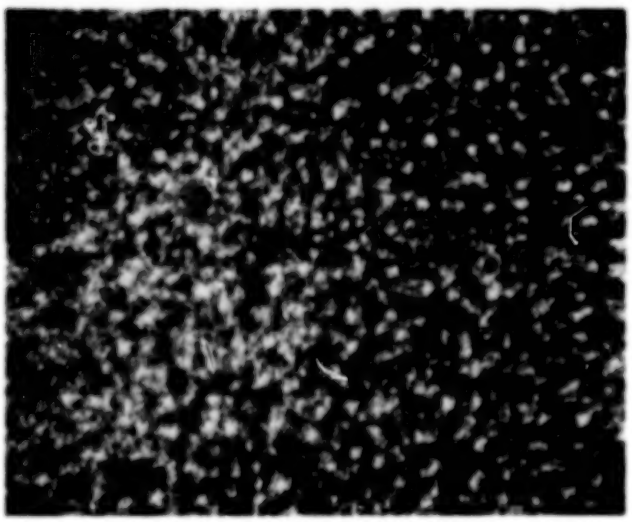
(a) Optical Photomicrograph (247X)



(b) $^{69}Ga^{+}$ Ion Micrograph (250X)

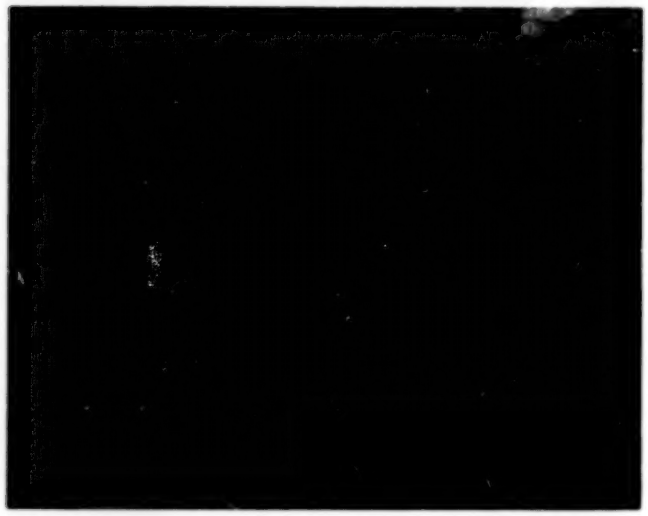
Figure 21. Interface Region of $GaAs_{0.5}P_{0.5}$ Steam Oxide

(c) $^{75}As^{+}$ Ion Micrograph (250X)

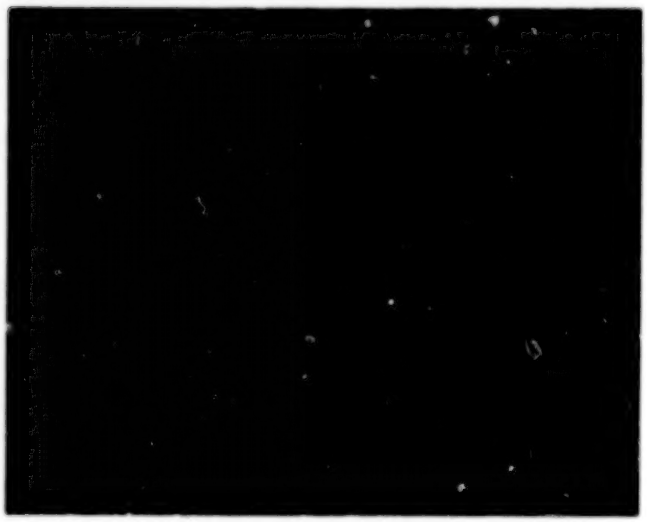


(d) $^{31}P^{+}$ Ion Micrograph (250X)

Figure 21. Interface Region of $GaAs_{0.5}P_{0.5}$ Steam Oxide



(e) $^{16}O^{+}$ Ion Micrograph (250X)



(f) $^{18}O^{+}$ Ion Micrograph (250X)

Figure 21. Interface Region of $GaAs_{0.5}P_{0.5}$ Steam Oxide

SECTION V

DIELECTRIC CHEMICAL AND ELECTRICAL STABILITY

This section describes the effects of bias and temperature stressing on both the electrical characteristics and ion microprobe depth profiles of $GaAs_{1-x}P_x$ MIS structures. The results of these measurements are correlated and some comments are made regarding the stability of the oxides thermally grown on $GaAs_{1-x}P_x$.

Bias-Temperature Stressing Experiments: C-V and IMMA Results

Figures 22(a) and (b) show the capacitance-voltage characteristics of an Ar-annealed $GaAs_{0.5}P_{0.5}$ MIS device before and after bias-temperature (B-T) stressing with positive and negative gate fields, respectively.

The magnitudes of the stress voltages used for these tests were chosen so that dielectric leakage currents were not significant enough to cause oxide breakdown problems. The stress temperature and time correspond to those commonly used in assessing the reliability and stability of MOS type semiconductor devices. As seen in Figure 22(a), the major effect of the positive B-T stress is a positive shift of about 2 volts, indicating possible electron injection and trapping. A reduction in hysteresis is also observed. The negative B-T stress has only a slight effect on the C-V characteristic, as shown in Figure 22(b). The rise in the capacitance at large negative voltage is not understood, but may be due to surface conduction. The corresponding ion microprobe depth profiles of these devices are shown in Figures 23(a) through (c). There are no noticeable changes in the IMMA profiles following stressing.

The "wide" aluminum-oxide interfaces of Figure 23 illustrate some of the knock-in effects of the IMMA technique described in the last section. The slightly higher aluminum count level towards the semiconductor bulk for the pre-stressed device of Figure 23(a) is not of significance, because this represents the noise level for this particular element.

Bias-temperature stressing effects on both unannealed and annealed lightly doped material were investigated. Figures 24(a) through (d) show the C-V characteristics of unannealed and Ar-annealed $GaAs_{0.5}P_{0.5}$ MIS devices before and after undergoing positive and negative B-T stressing. The unannealed devices again show reduced hysteresis after both the positive and negative

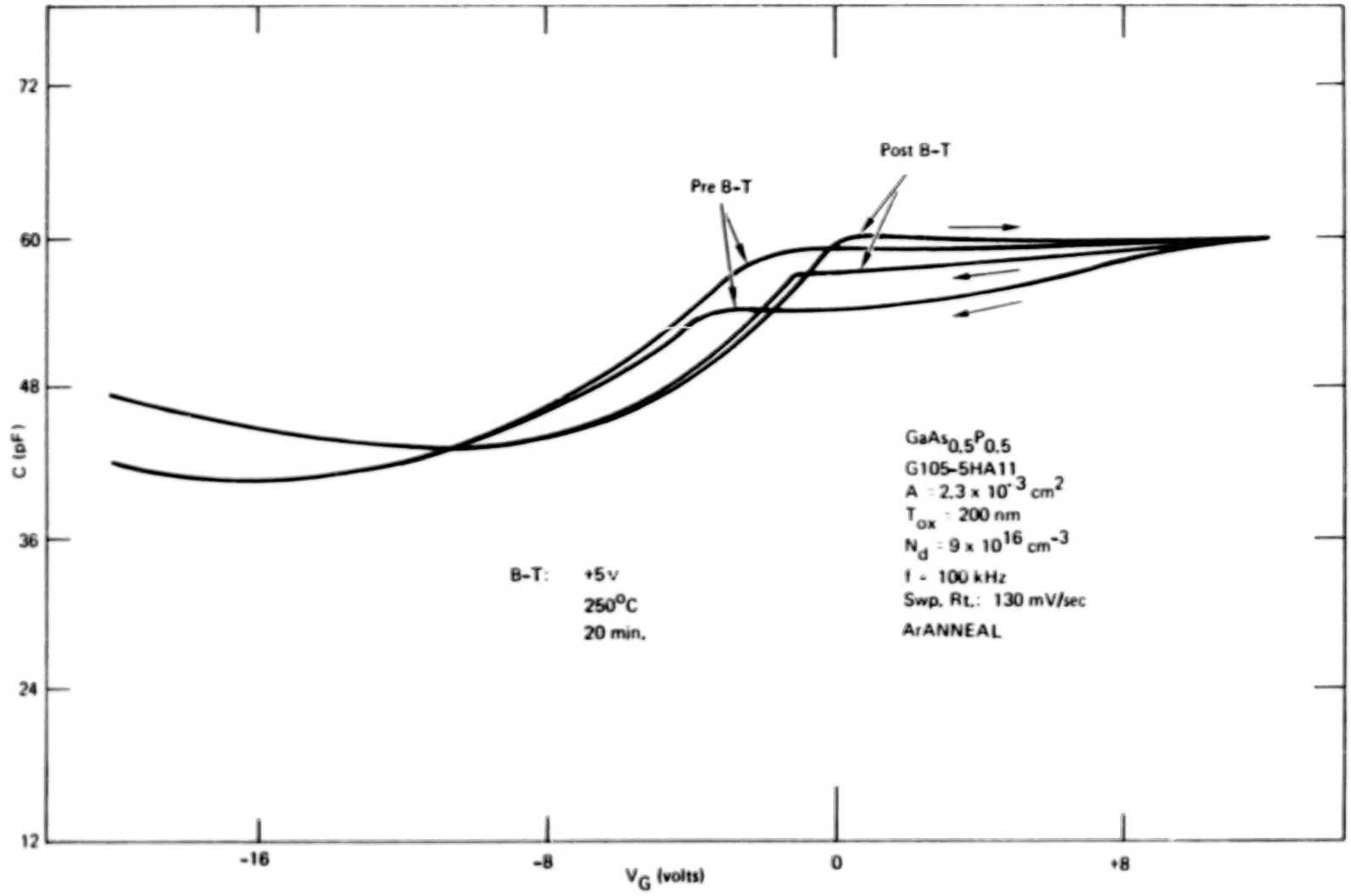


Figure 22(a). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristic Before and After Positive Bias-Temperature Stress

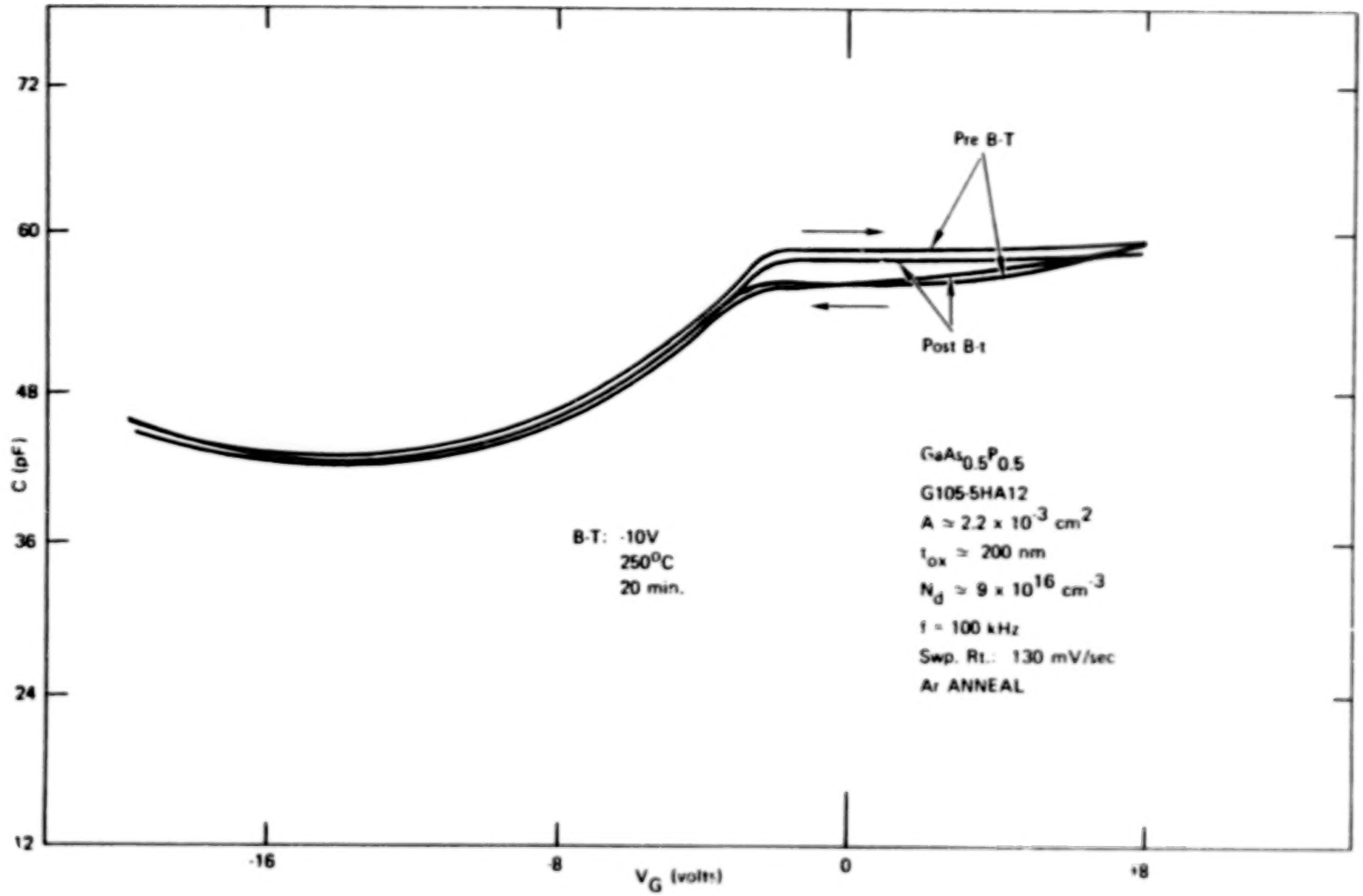


Figure 22(b). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristics Before and After Negative Bias-Temperature Stress

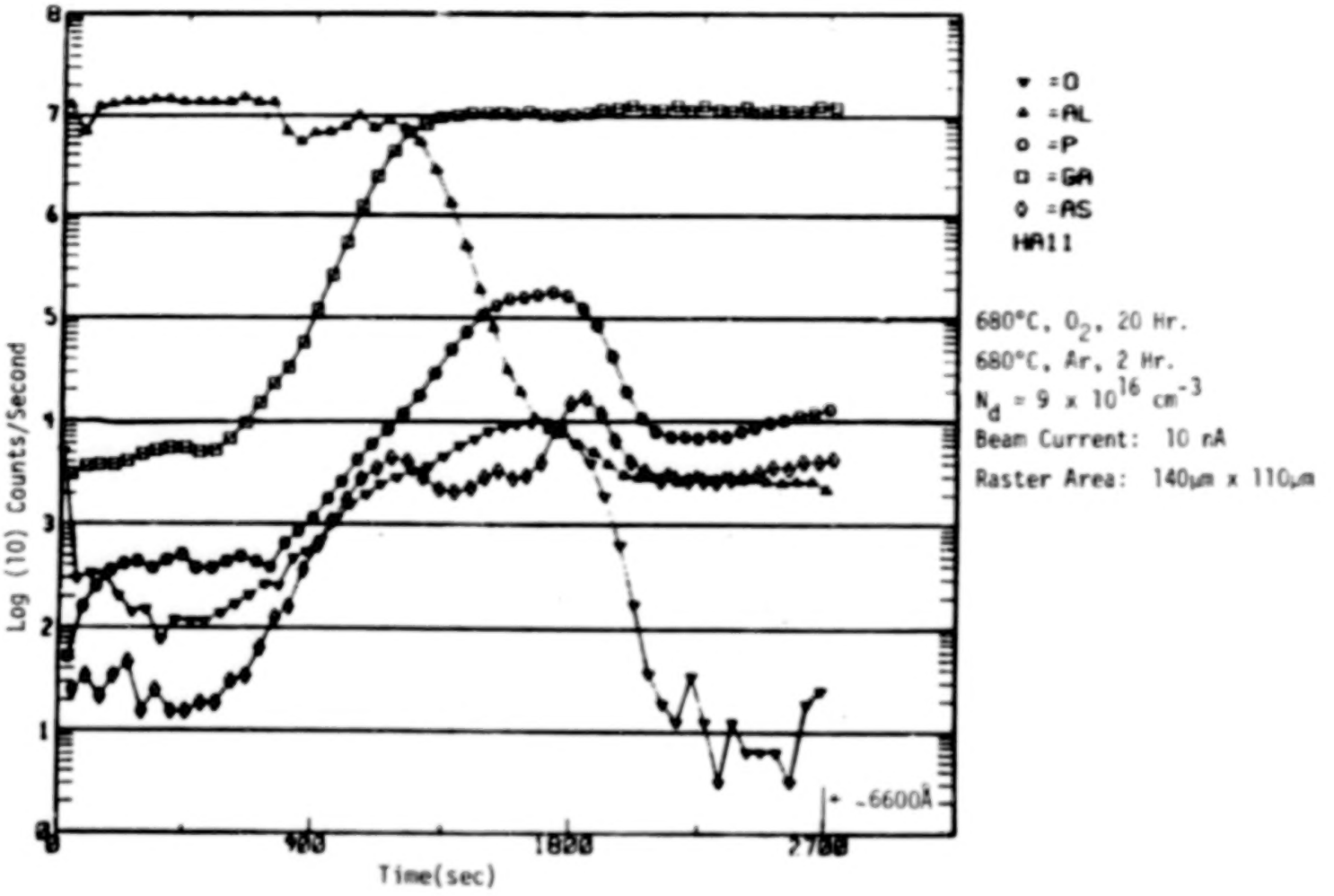


Figure 23(a). IMMA Profile of $GaAs_{0.5}P_{0.5}$ MIS Structure Before B-T Stress (Ar-Annealed)

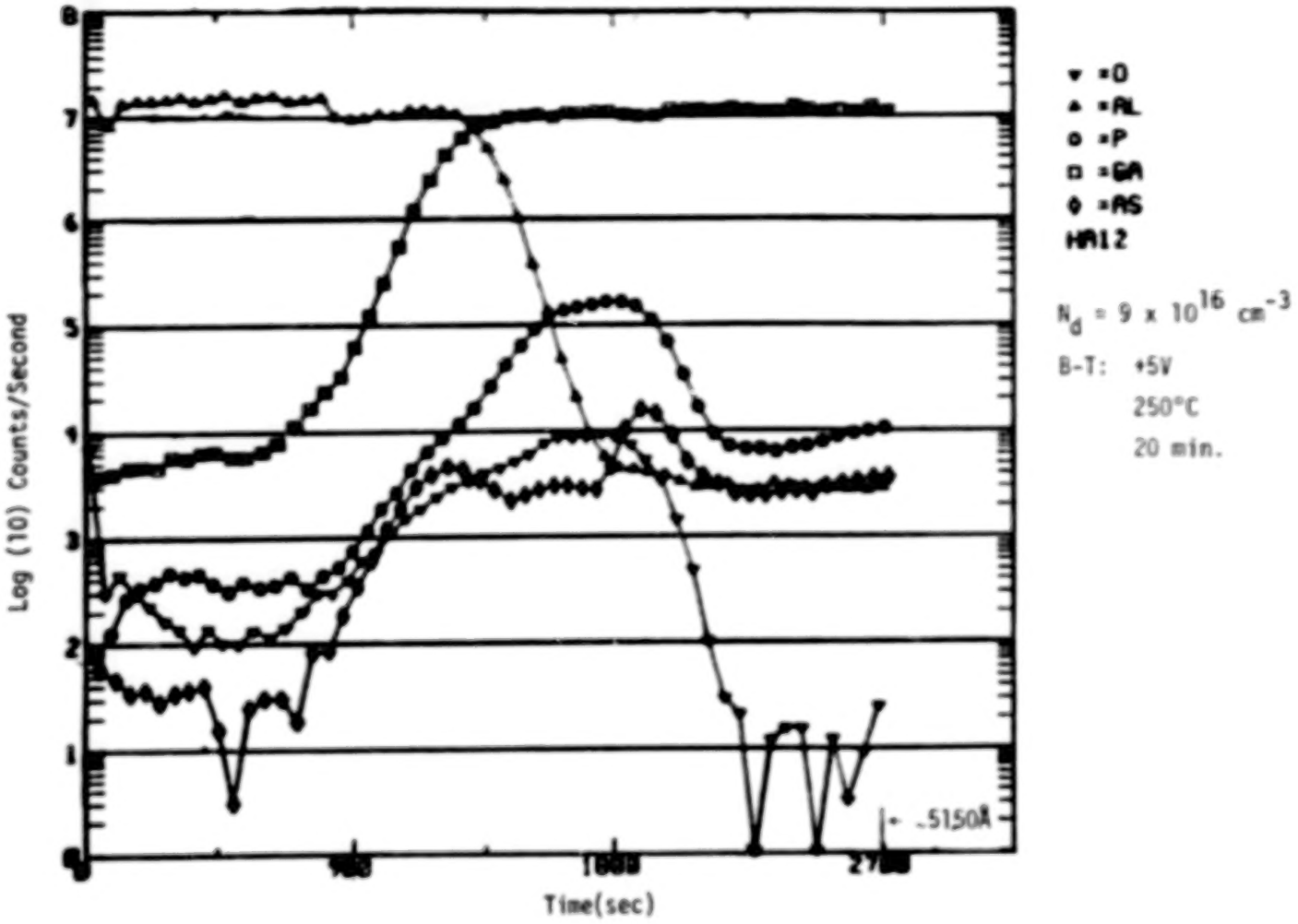


Figure 23(b). IMMA Profile of $GaAs_{0.5}P_{0.5}$ MIS Structure After Positive B-T Stress

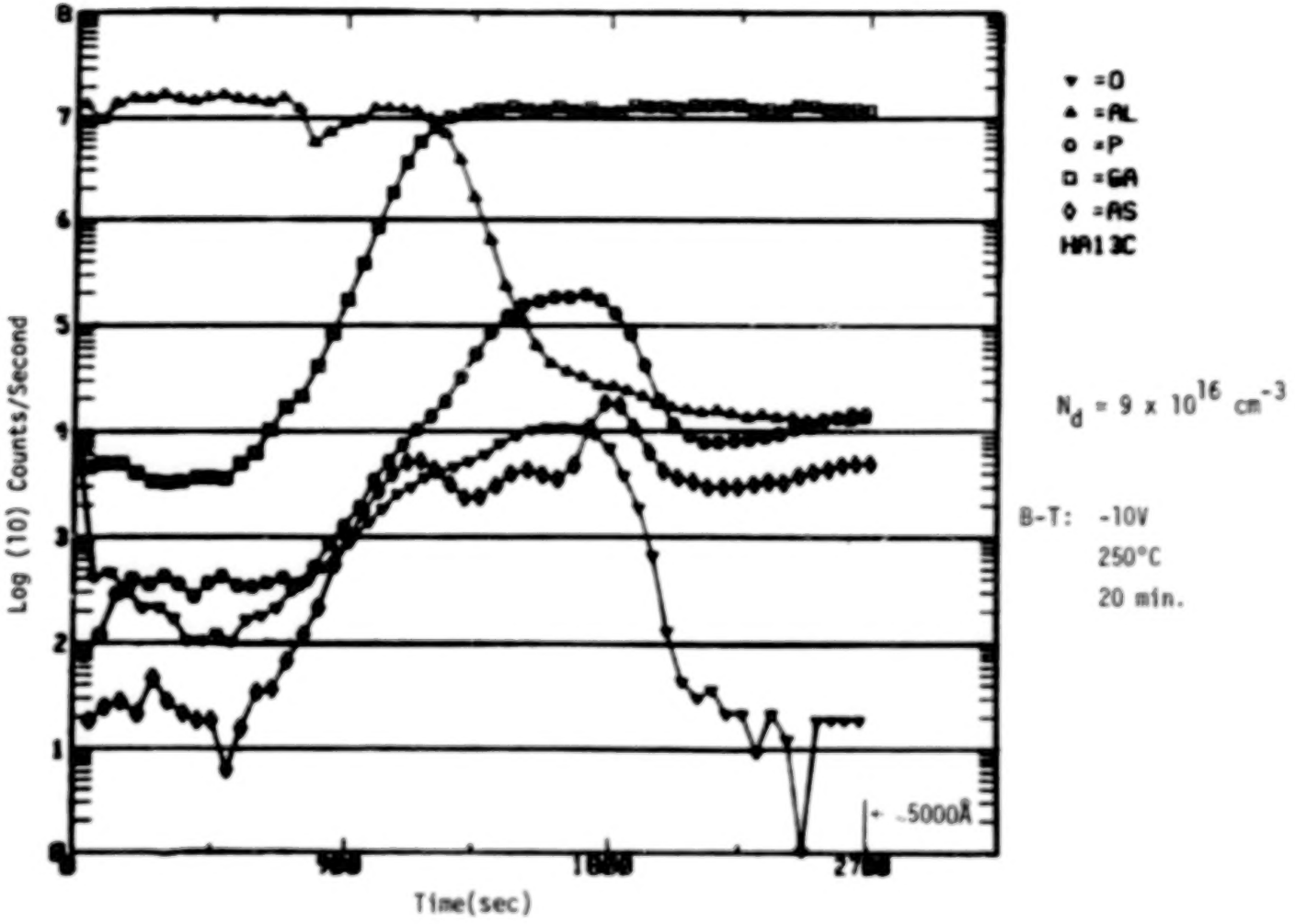


Figure 23(c). IMMA Profile of $GaAs_{0.5}P_{0.5}$ MIS Structure After Negative B-T Stress

stressing. The annealed devices show no major changes in the magnitude of the hysteresis, but only small shifts of the curves in the positive direction.

The IMMA profiles corresponding to the characteristics of Figure 24 are shown in Figures 25(a) through (f). Comparison of the profiles for the unannealed samples [Figures 25(a) - (c)] shows that there are no major changes caused by the stressing. The increase in the aluminum count starting at about 1400 sec. in Figure 25(a) may have been due to a temporary error in the data reduction scheme, but no anomalies are observed for the other elements.

Profiles of the Ar-annealed samples [Figures 25(d) - (f)] show some variations in the leading edge of the phosphorus profiles for the different stressing conditions. These variations probably are not of significance because they were not observed on the other samples [Figures 23(a) - (c)] and Figures 25(a) - (c)]. There is a very slight reduction in the maximum count level of the arsenic peak nearest the oxide surface for the positive voltage stressed sample relative to the unstressed sample. It is believed that this reduction is due more to a slightly lower sputtering rate than to a real change in the elemental composition caused by the stressing conditions.

Although the bias-temperature stressing conditions used here do not cause any significant changes in the elemental oxide profiles, a comparison of the profiles for the annealed and unannealed devices shows that the maximum level of the surface arsenic peak is lower relative to the leading edge of the phosphorus peak for the annealed samples. This behavior is consistent with that demonstrated by the profiles in Figure 18 for $GaAs_{0.6}P_{0.4}$ dry oxides.

The Ar-annealed profiles of Figures 23 and 25(d) - (f) for the heavily and more lightly-doped structures displayed the same general features (i.e., a low-level surface and high-level interface arsenic peak). However, the rather broad constant arsenic level in the central portion of the oxides of Figure 23 is distinctly different compared to the well-defined minimum in Figures 25(d) - (f). This difference is not understood, since all oxides were grown during the same oxidation run, and differences in the impurity level are not expected to result in changes in the thermal oxidation kinetics. However, the impurity doping levels do affect the kinetics of GaAs anodic oxidation. Such compositional differences may be able to partially account for the anomalies in electrical characteristics described earlier (Section IV).

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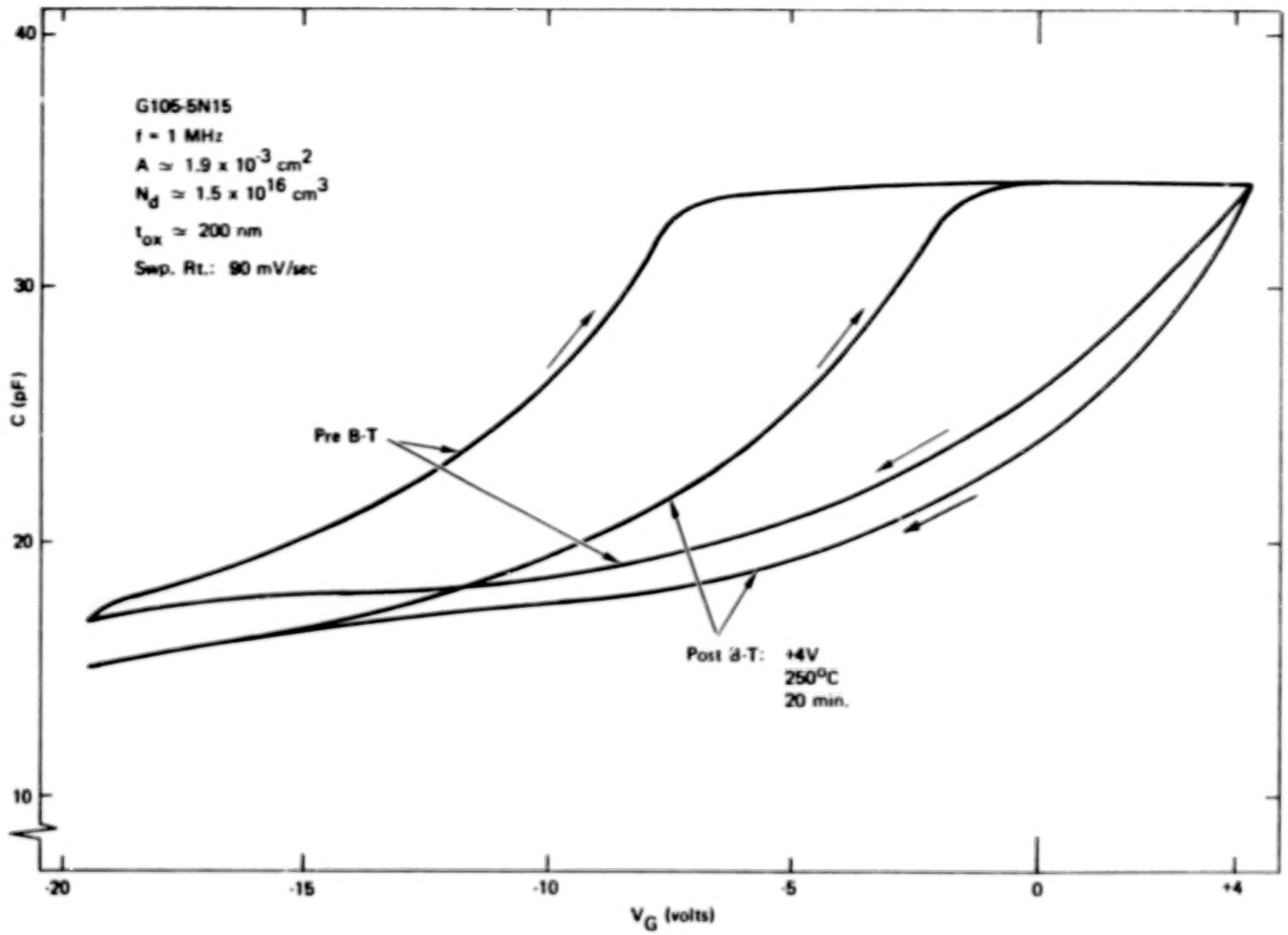

Figure 24(a). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristic Before and After Positive B-T Stress (Unannealed)

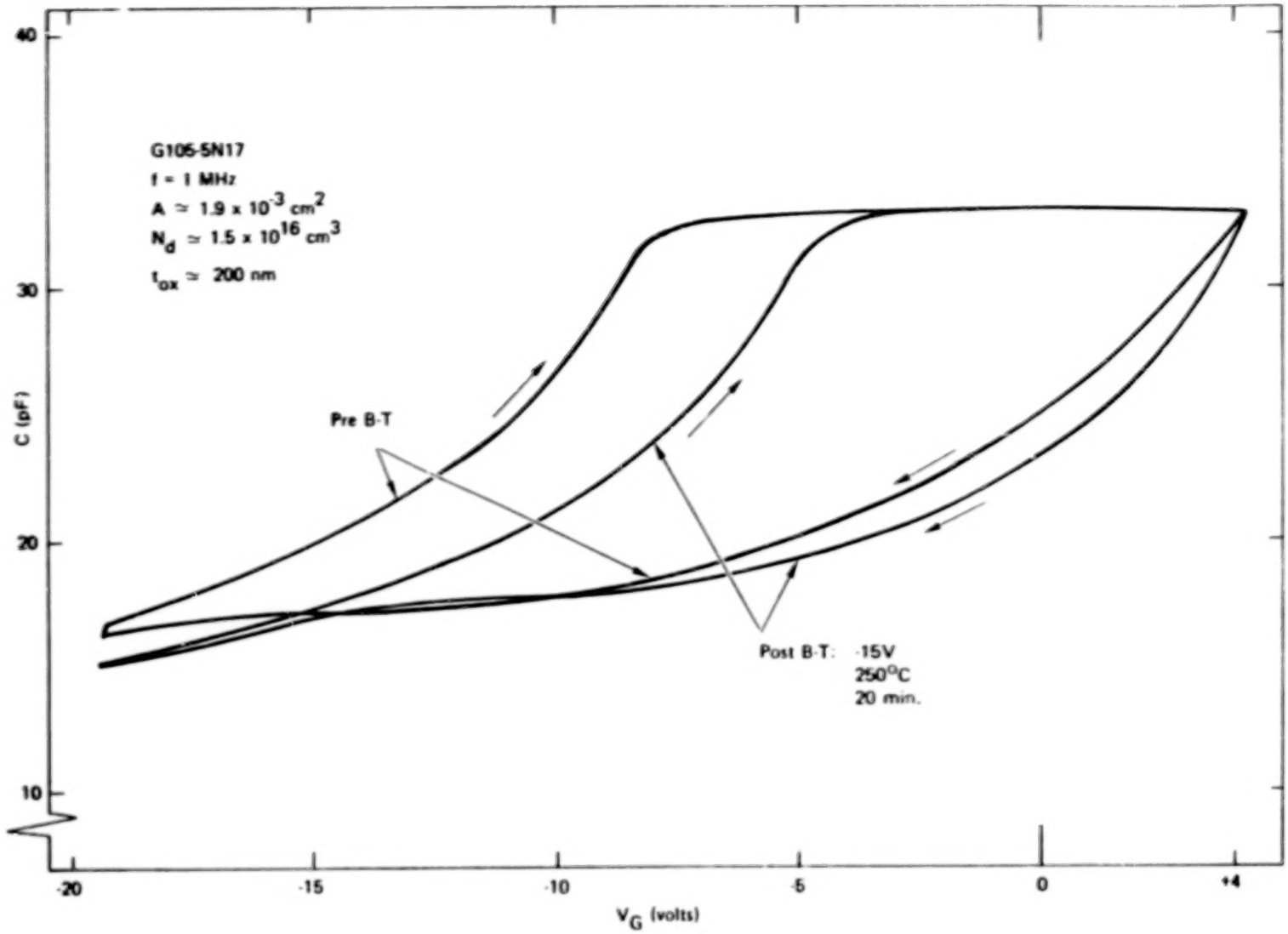

Figure 24(b). $GaAs_{0.5}P_{0.5}$ C-V Characteristic Before and After Negative B-T Stress (Unannealed)

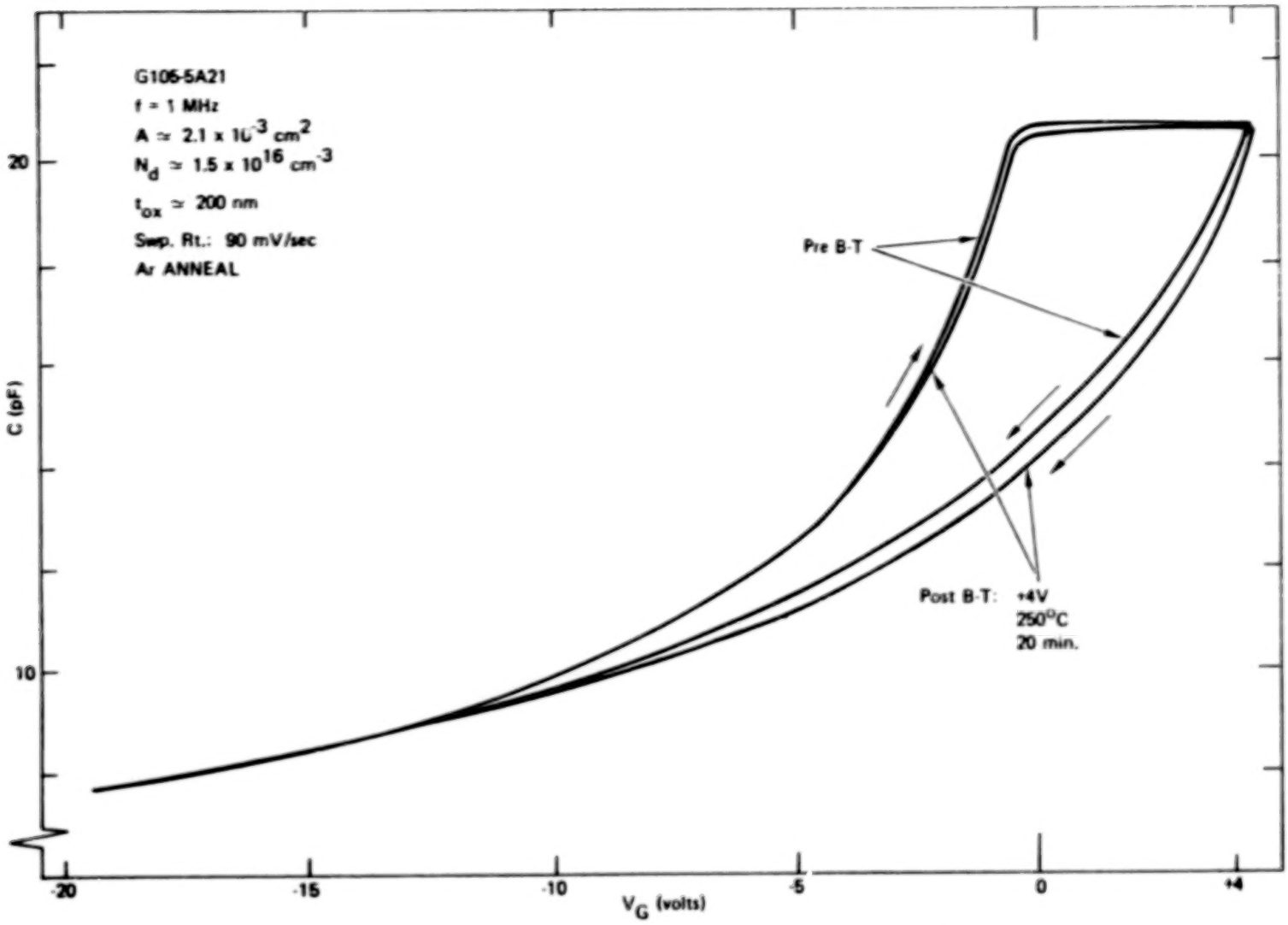

Figure 24(c). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristic Before and After Positive B-T Stress (Ar-Annealed)

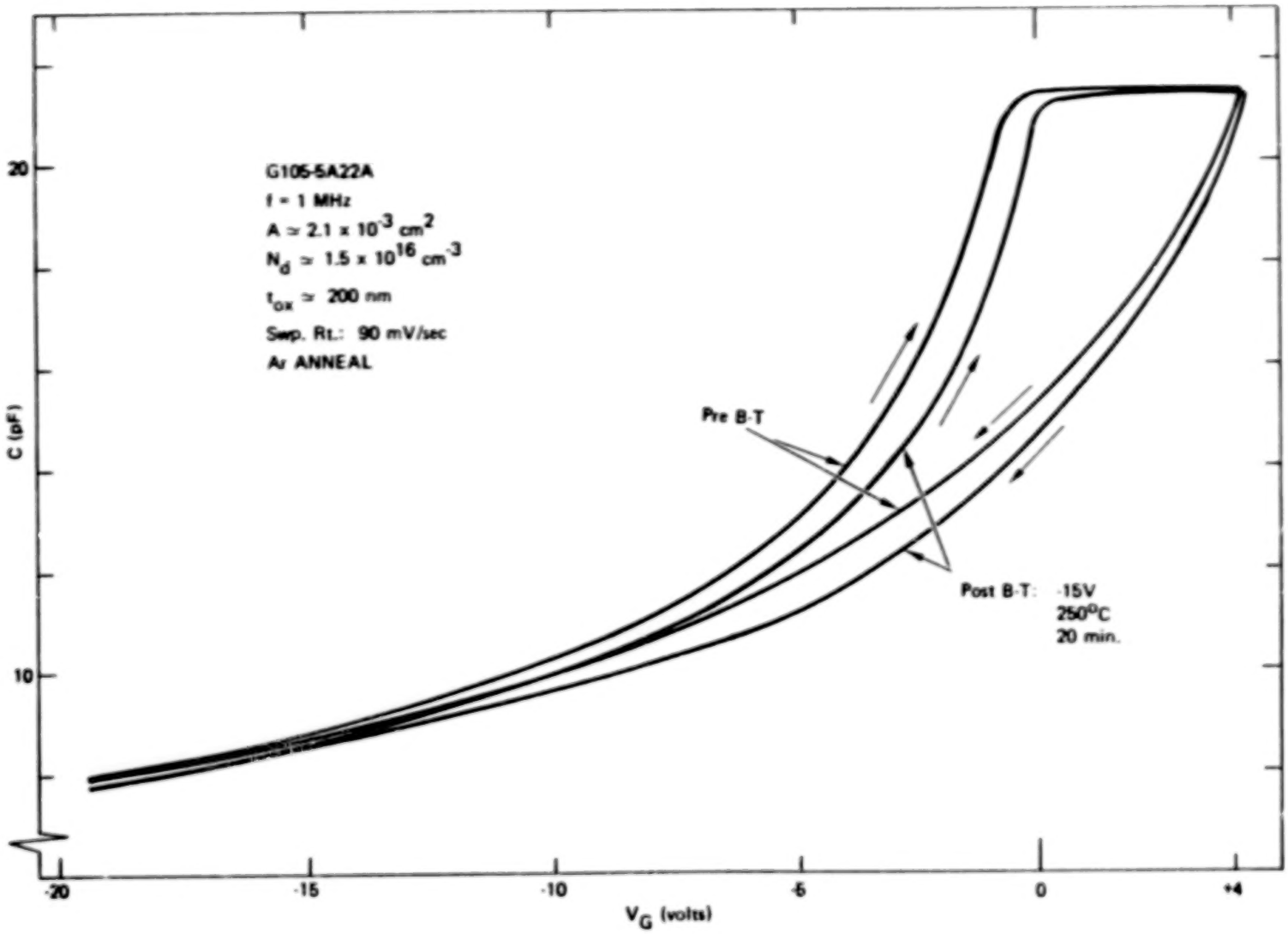

Figure 24(d). $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristic Before and After Negative B-T Stress (Ar-Annealed)

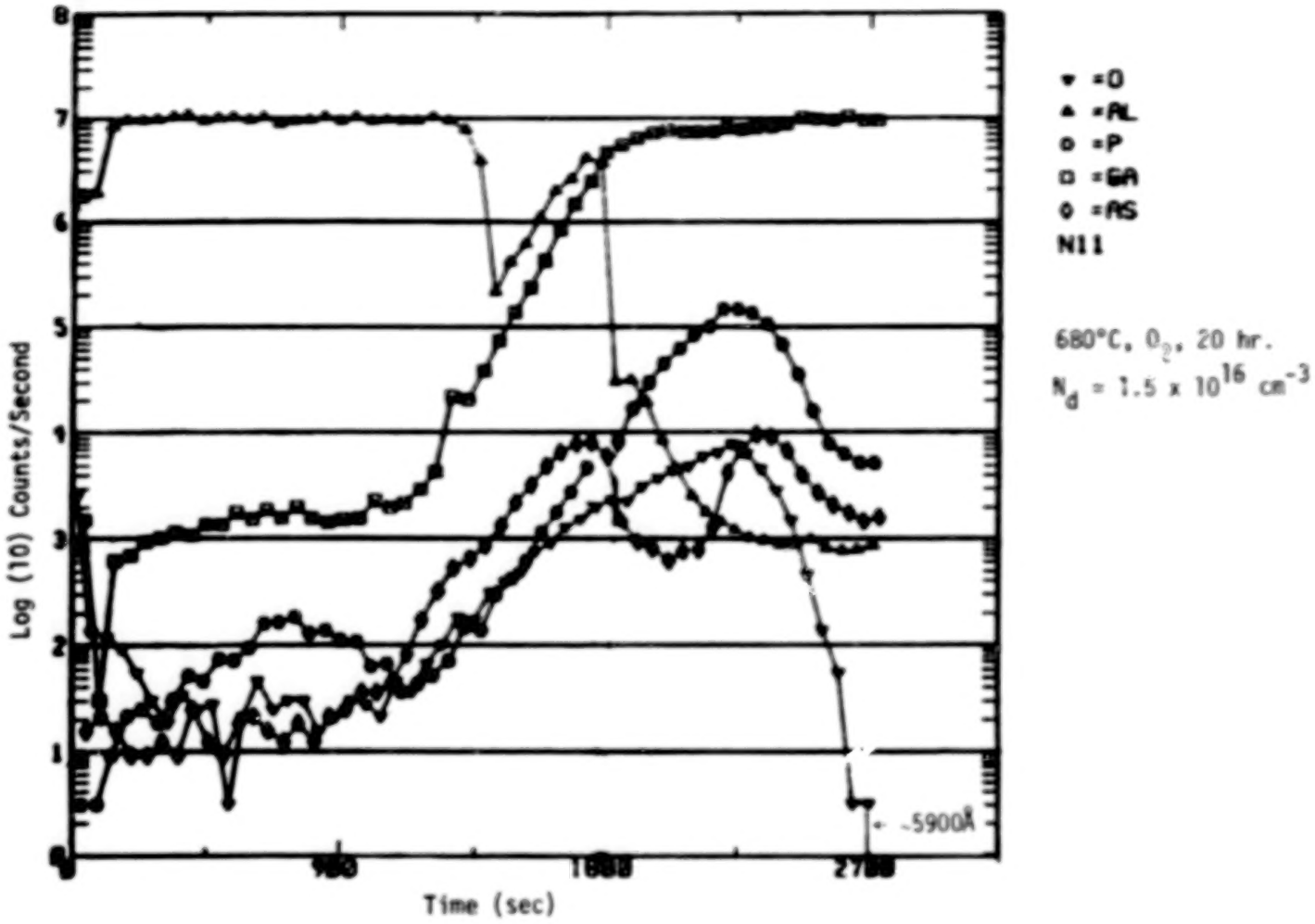

Figure 25(a). IMMA Profile of Unannealed $GaAs_{0.5}P_{0.5}$ MIS Device Before B-T Stressing

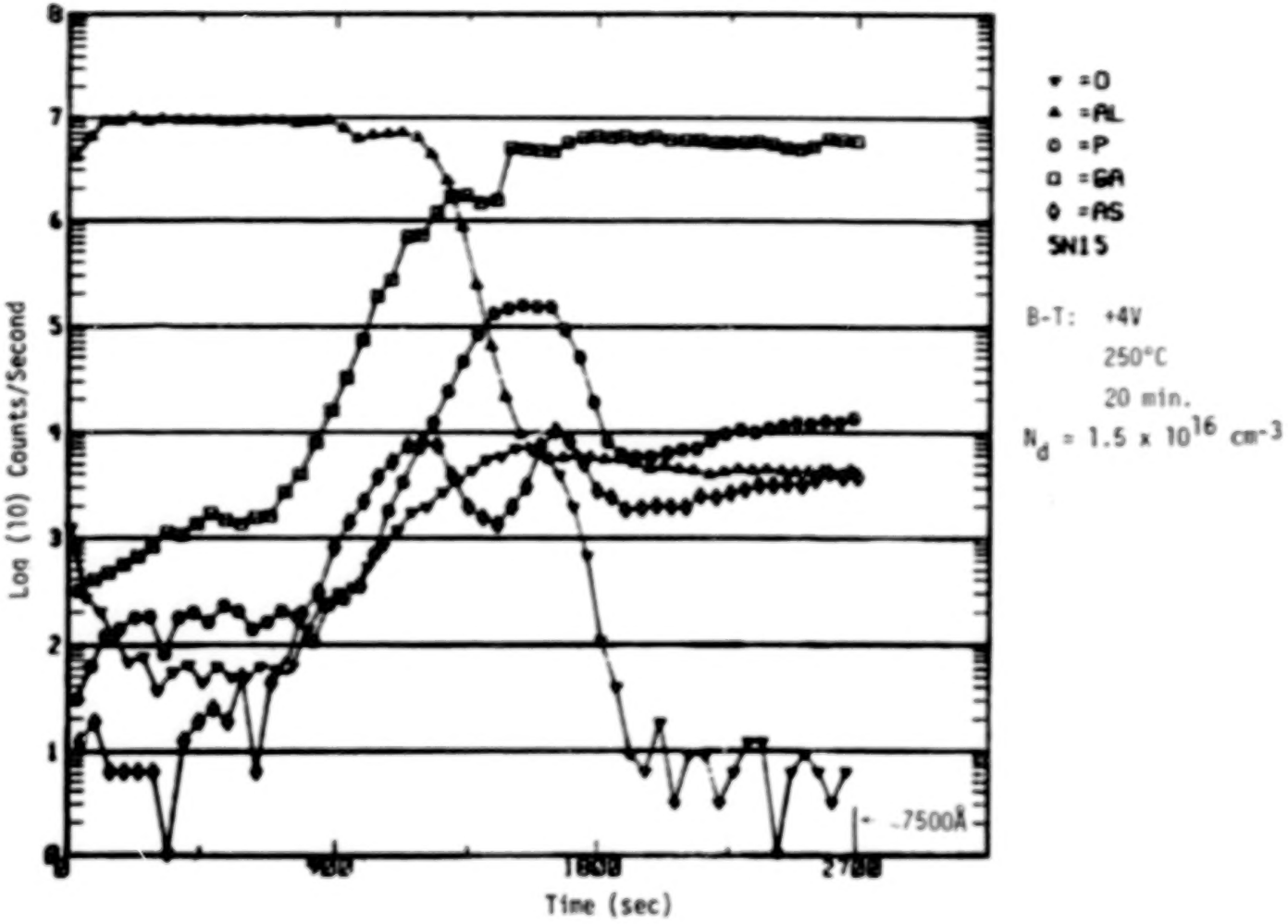

Figure 25(b). IMMA Profile of Unannealed $GaAs_{0.5}P_{0.5}$ MIS Device Following Positive B-T stress

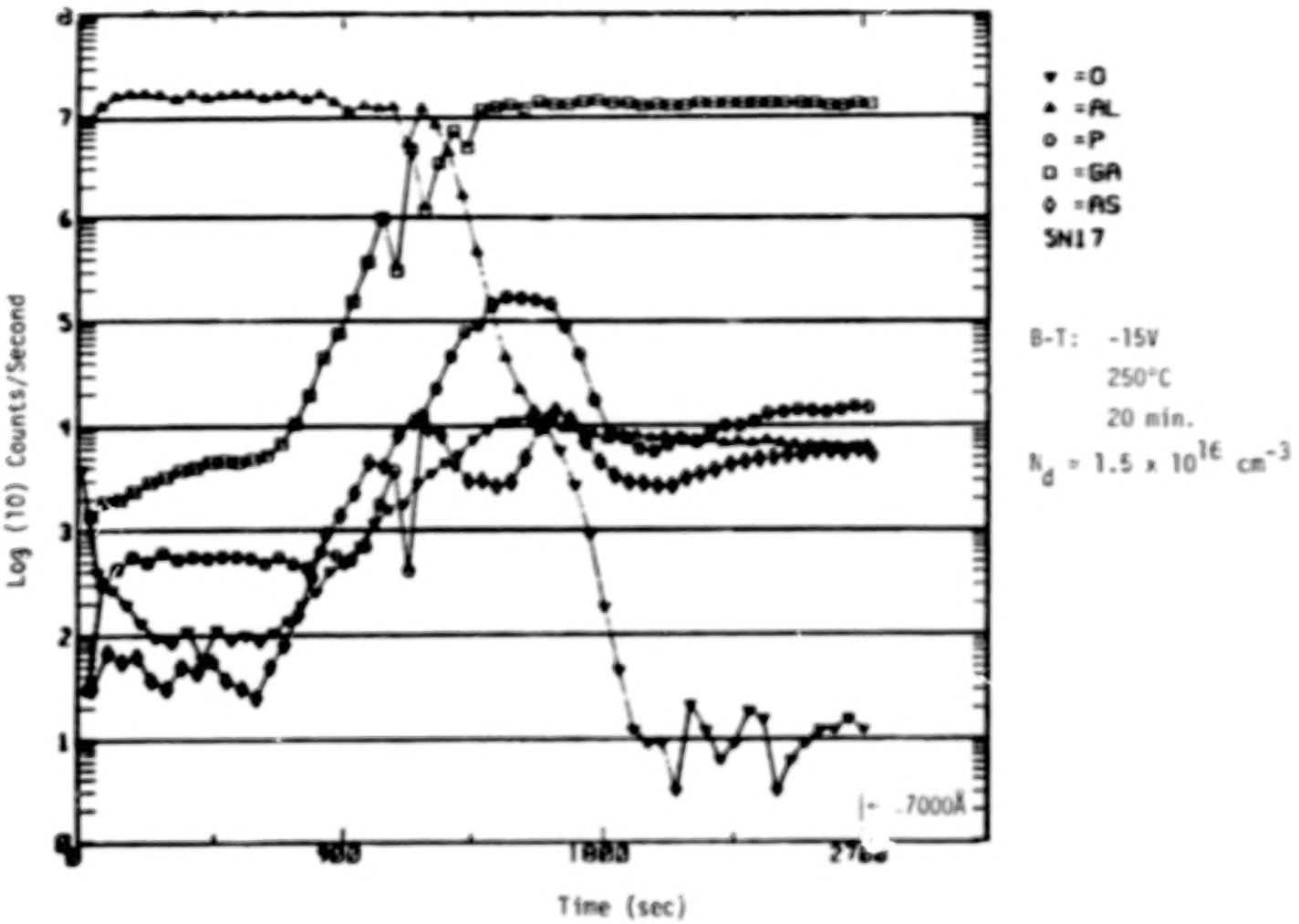

Figure 25(c). IMNA Profile of Unannealed $GaAs_{0.5}P_{0.5}$ M'S Device Following Negative B-T Stress

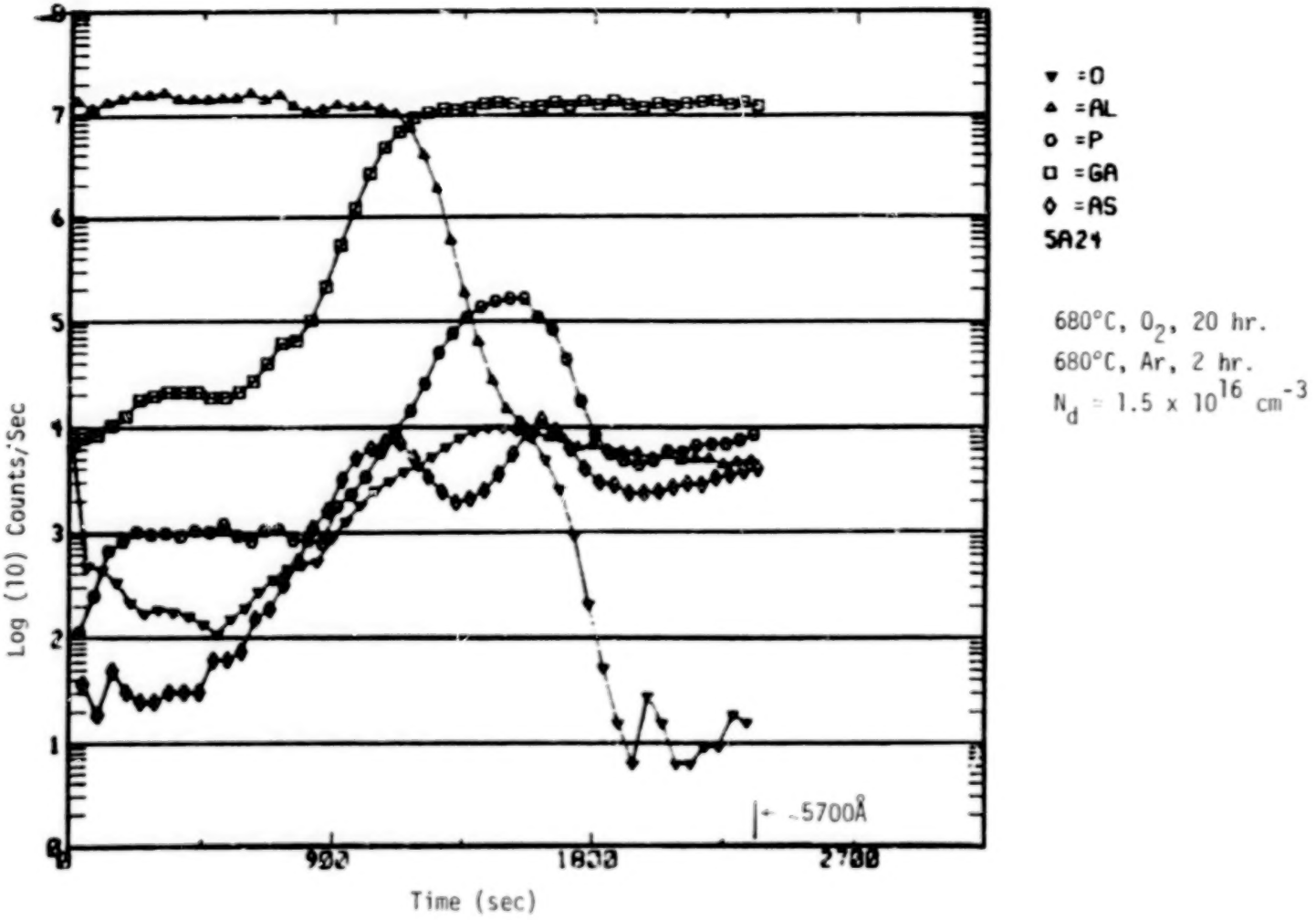

Figure 25(d). IMMA Profile of Ar-Annealed $GaAs_{0.5}P_{0.5}$ MIS Device Before B-T Stressing

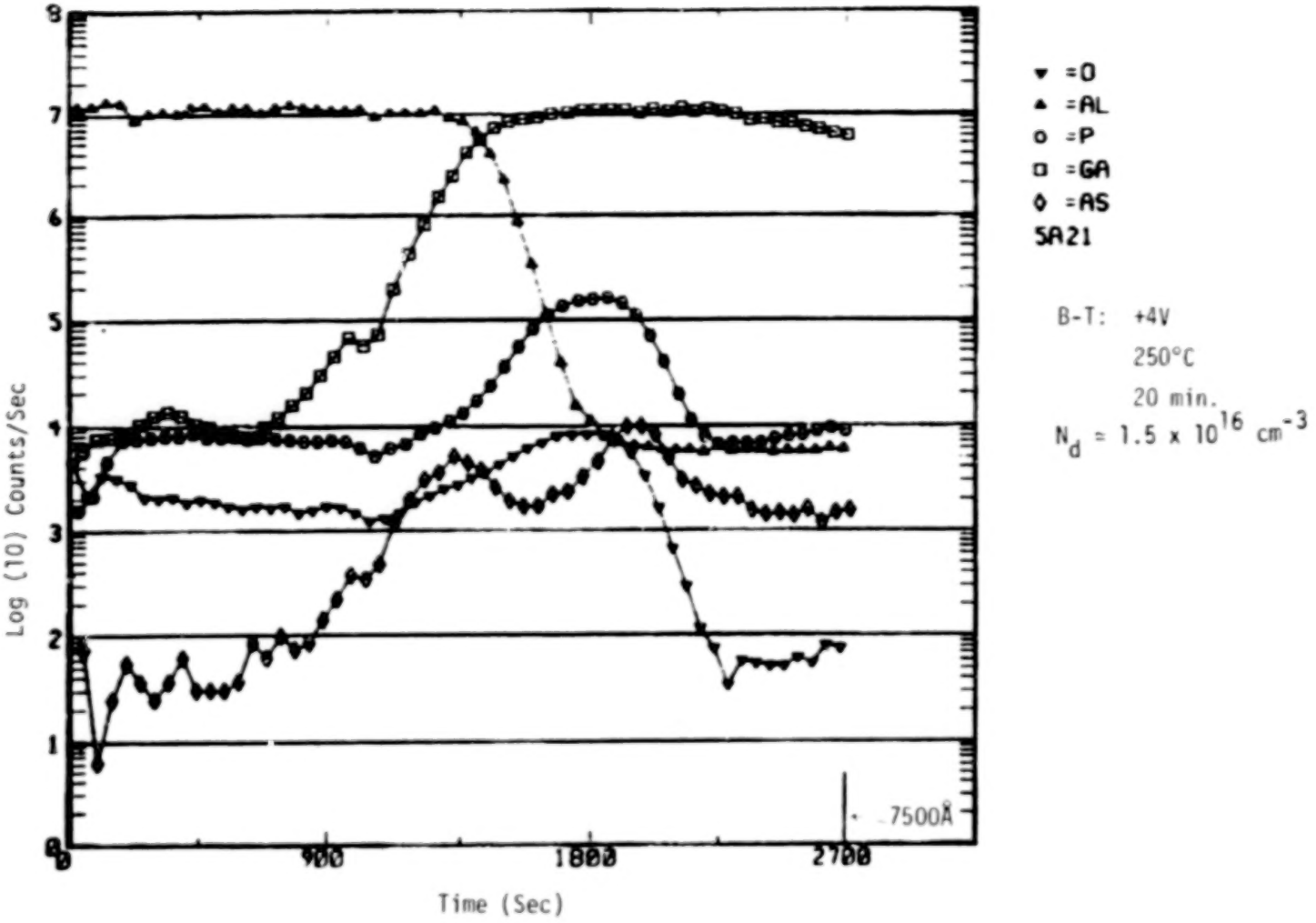

Figure 25(e). IMMA Profile of Ar-Annealed $GaAs_{0.5}P_{0.5}$ MIS Device Following Positive B-T Stressing

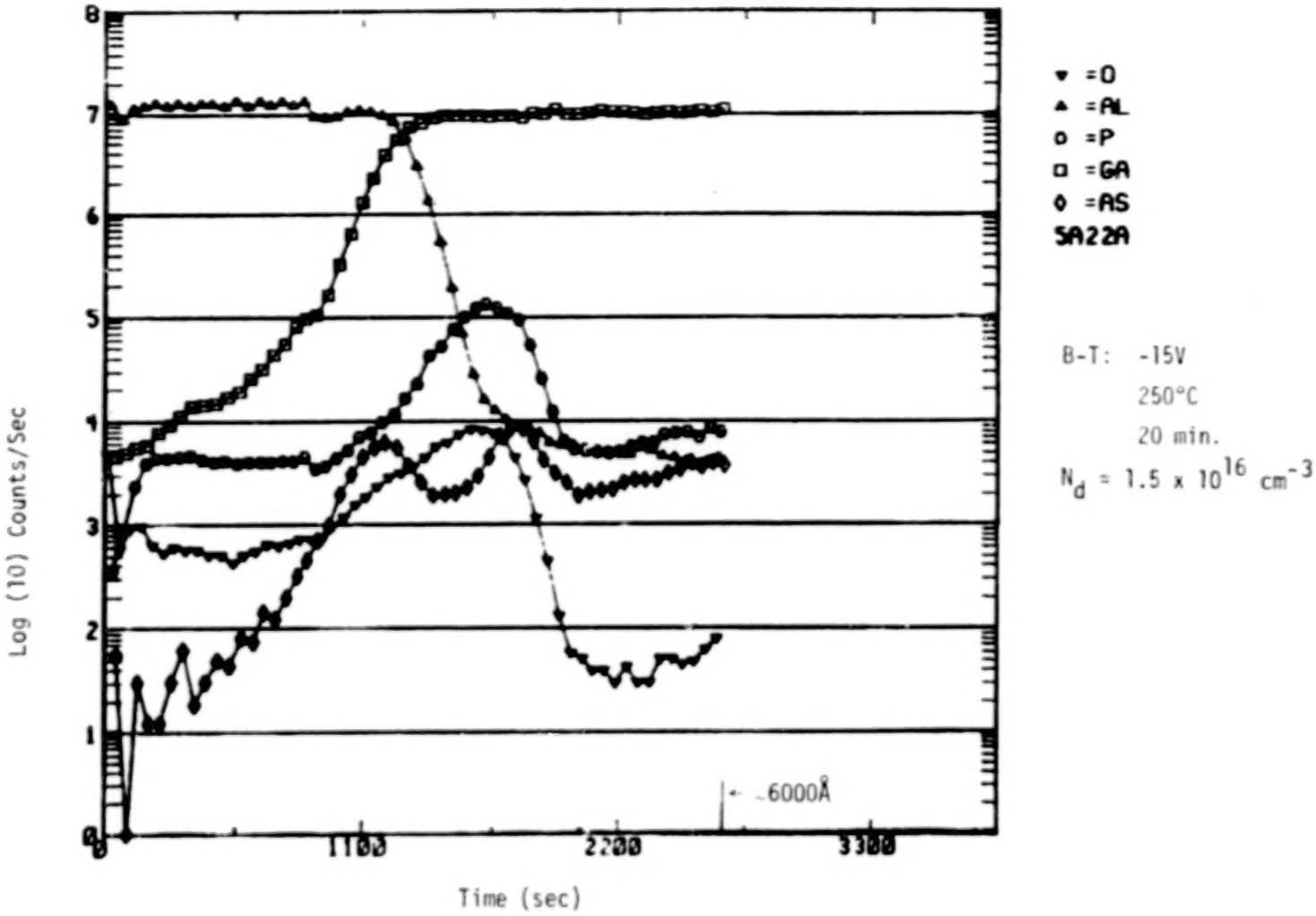

Figure 25(f). IMMA Profile of Ar-Annealed $GaAs_{0.5}P_{0.5}$ MIS Device Following Negative B-T Stressing

$GaAs_{0.6}P_{0.4}$ MIS devices also exhibited reduced hysteresis following B-T stress, lower surface arsenic levels for annealed devices, and no IMMA profile changes for stressed devices. Examples of $GaAs_{0.6}P_{0.4}$ MIS C-V characteristics and IMMA profiles are shown in Figures 26 and 27(a) - (c). The post-bias-temperature-stressed C-V curve in Figure 26 exhibits a reduction in capacitance from that of the unstressed curve. This effect was observed in certain cases on both $GaAs_{0.6}P_{0.4}$ and $GaAs_{0.5}P_{0.5}$ devices. The reduction may be due to changes in the properties of the dielectric with stressing, or to a contact problem, although manipulation of the device with the probe could not restore the original capacitance values. In any case, the depth profiles do not show shifts that would indicate a change in the dielectric composition.

Additional Bias-Temperature Stressing Effects

Dielectric Leakage -- As mentioned in a previous section, reduced hysteresis in C-V characteristics is generally accompanied by a slight increase in dielectric leakage. Figure 28 shows the effect of a positive B-T stress on the current-voltage characteristics of an unannealed $GaAs_{0.5}P_{0.5}$ device. Figure 29 is the corresponding C-V characteristic of the same structure. It is seen that the slight increase in leakage current is associated with a slight reduction in C-V hysteresis. However, the physical change responsible for these effects are apparently too subtle for detection in the ion microprobe, as mentioned earlier.

Mobile Ion Contamination -- The major effects of stressing which have been observed suggest possible changes in the electron trapping properties of the oxide-semiconductor interface region as being responsible for changes in the electrical characteristics.

To determine if mobile ions are a major factor in device stability, some devices were purposely contaminated with a saturated salt water solution to introduce sodium ions to the oxide surface. The devices were then stressed and the resulting C-V characteristics showed no difference from those of uncontaminated devices. These results indicate that the major stability factor for these present devices is probably electron trapping effects. Ions other than sodium may result in detectable instability effects, however.

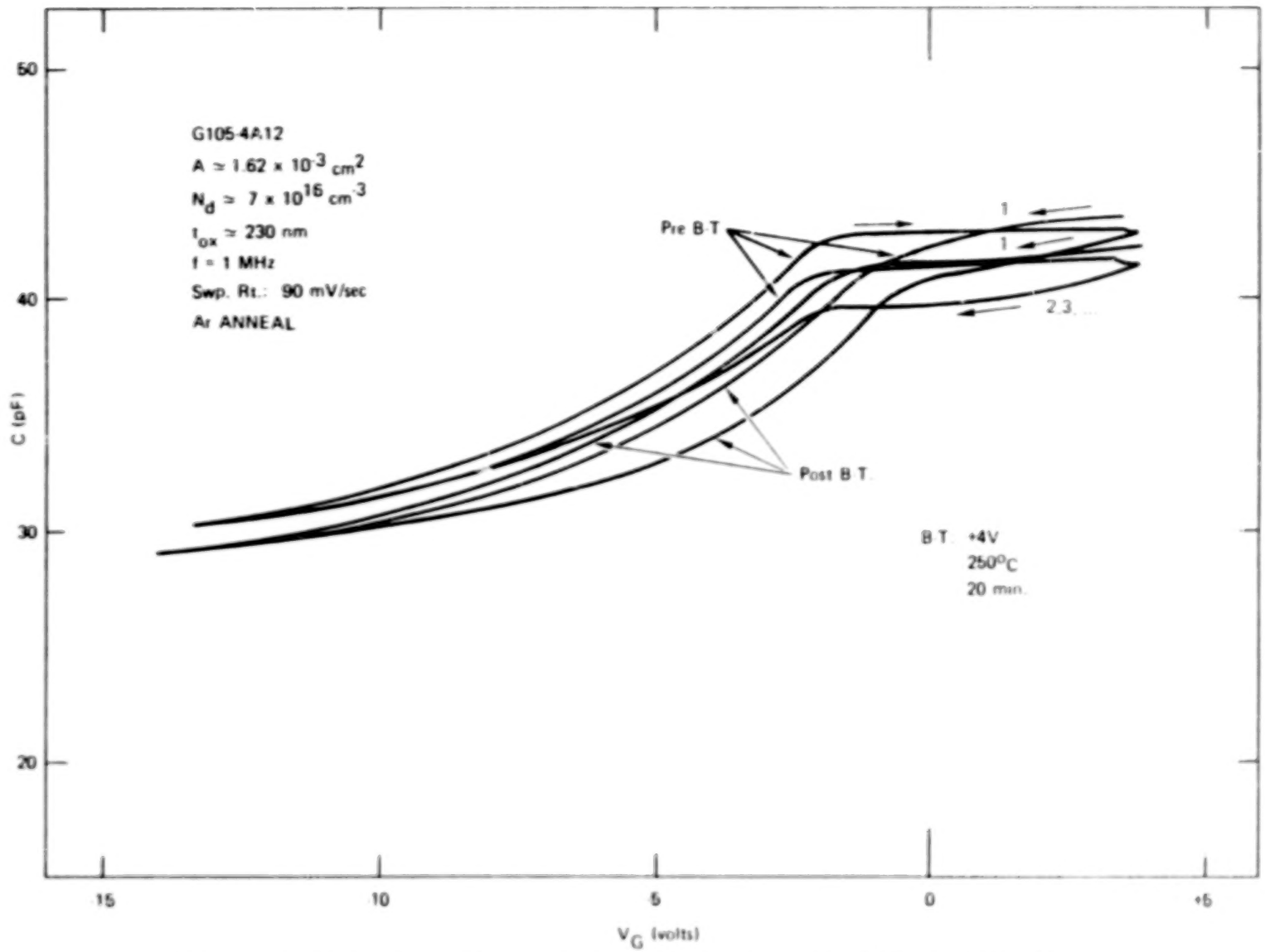

Figure 26. $GaAs_{0.6}P_{0.4}$ MIS C-V Characteristic Before and After B-T Stressing

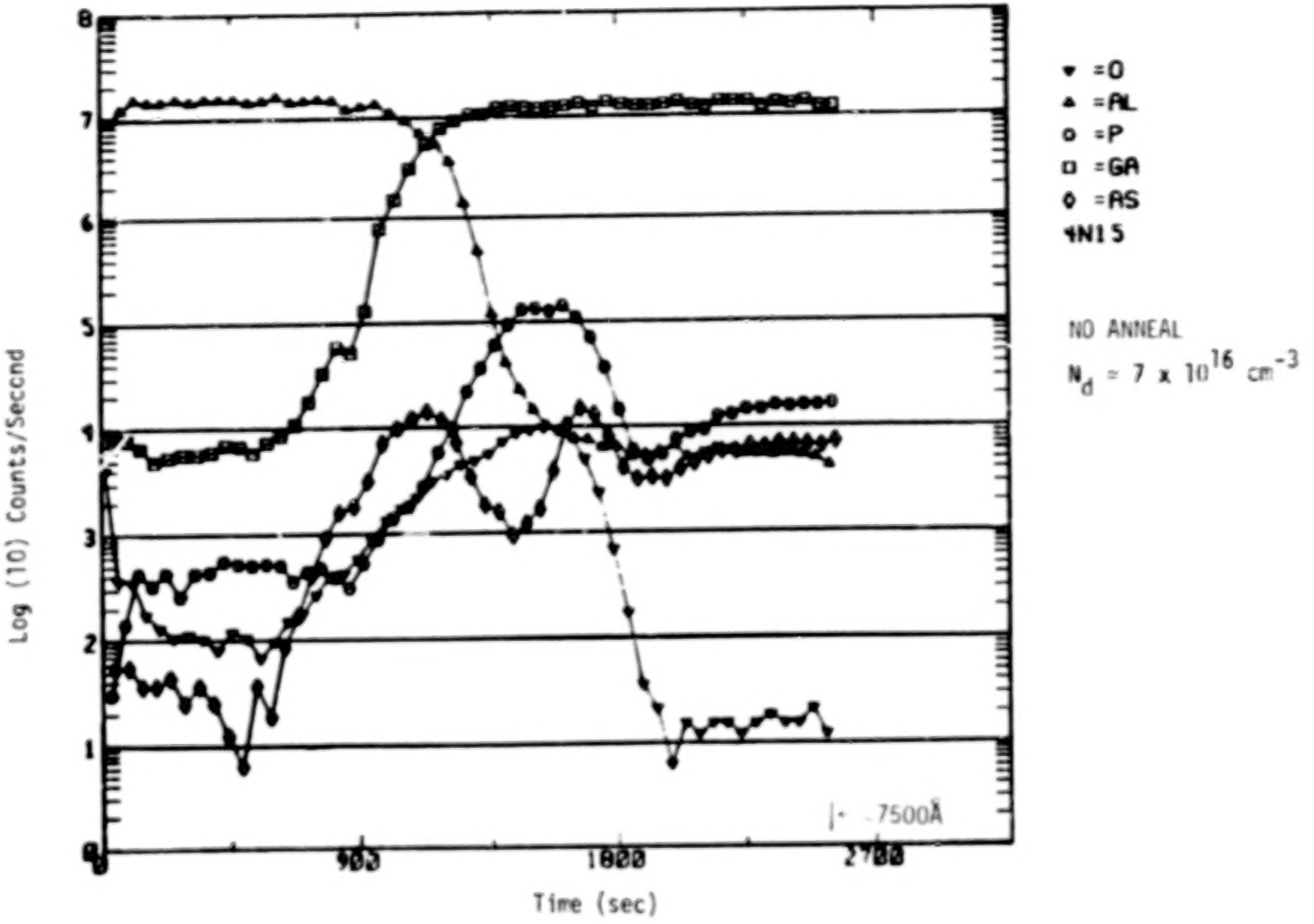

Figure 27(a). IMMA Profile of $GaAs_{0.6}P_{0.4}$ MIS Device Before B-T Stressing

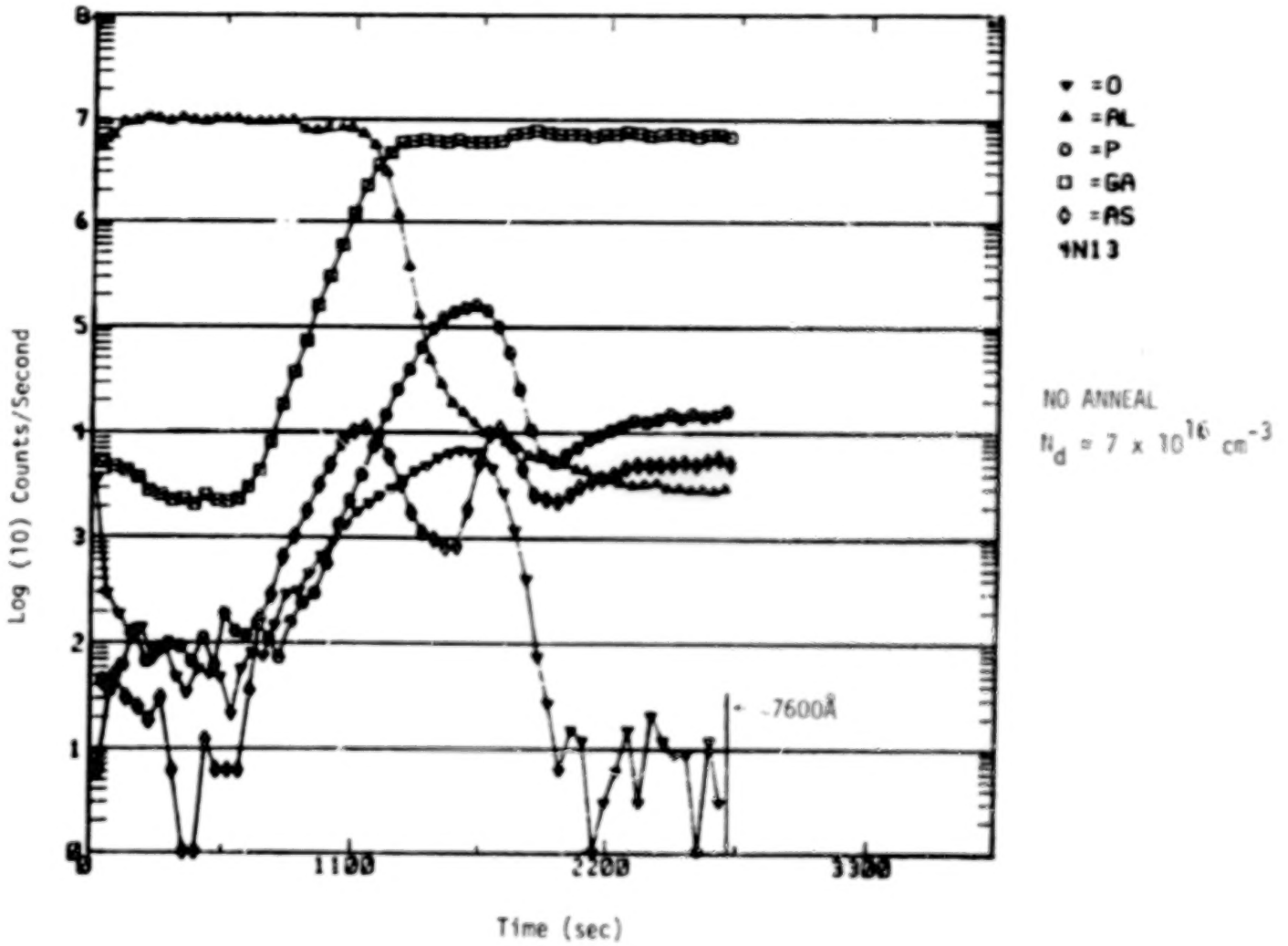

Figure 27(b). IMMA Depth Profile of $GaAs_{0.6}P_{0.4}$ MIS Device After Negative B-T Stressing

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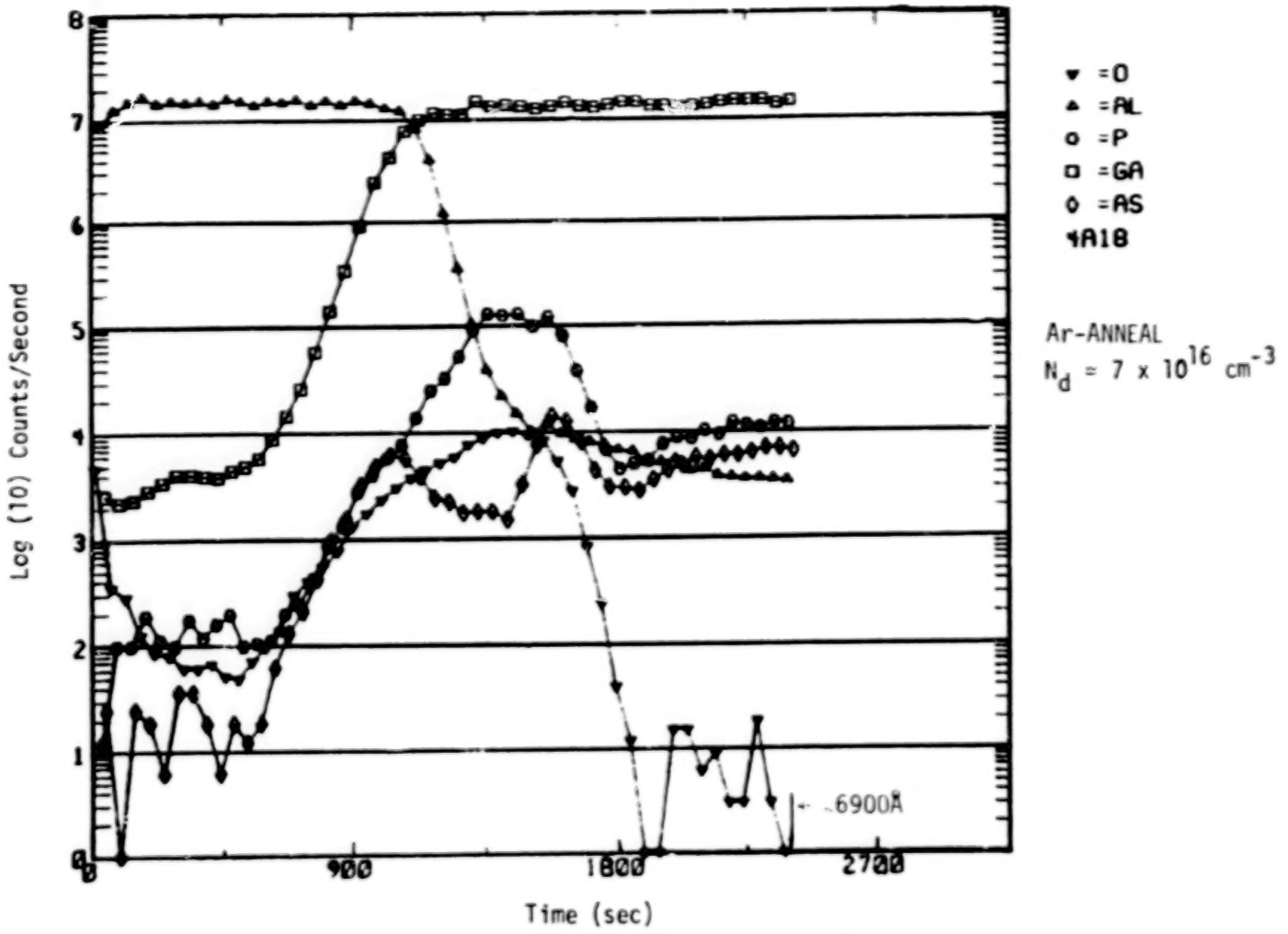

Figure 27(c). IMA Profile of $GaAs_{0.6}P_{0.4}$ MIS Device Before B-T Stressing

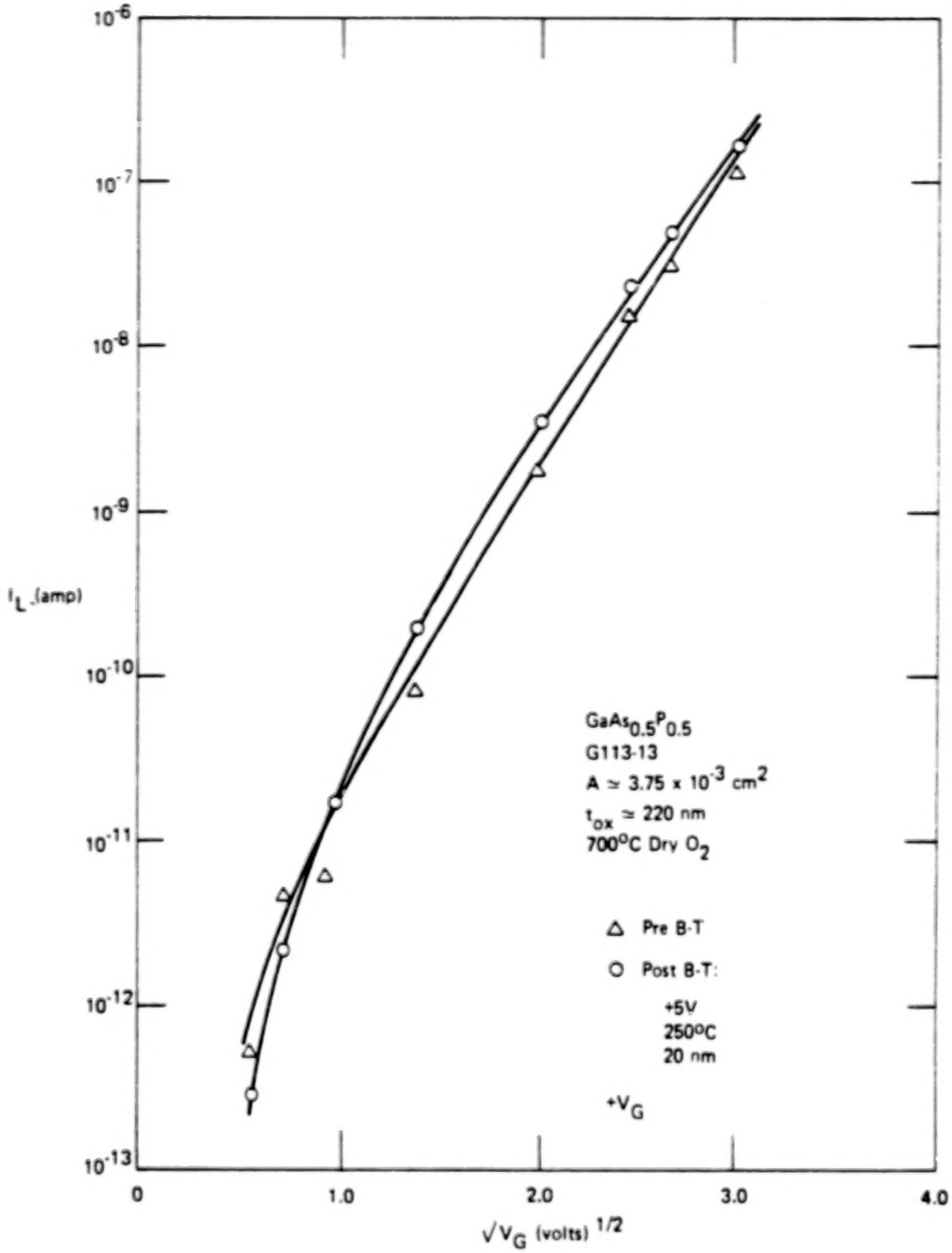

Figure 28. Effect of Bias-Temperature Stressing on I-V Characteristics of $GaAs_{0.5}P_{0.5}$ MIS Device

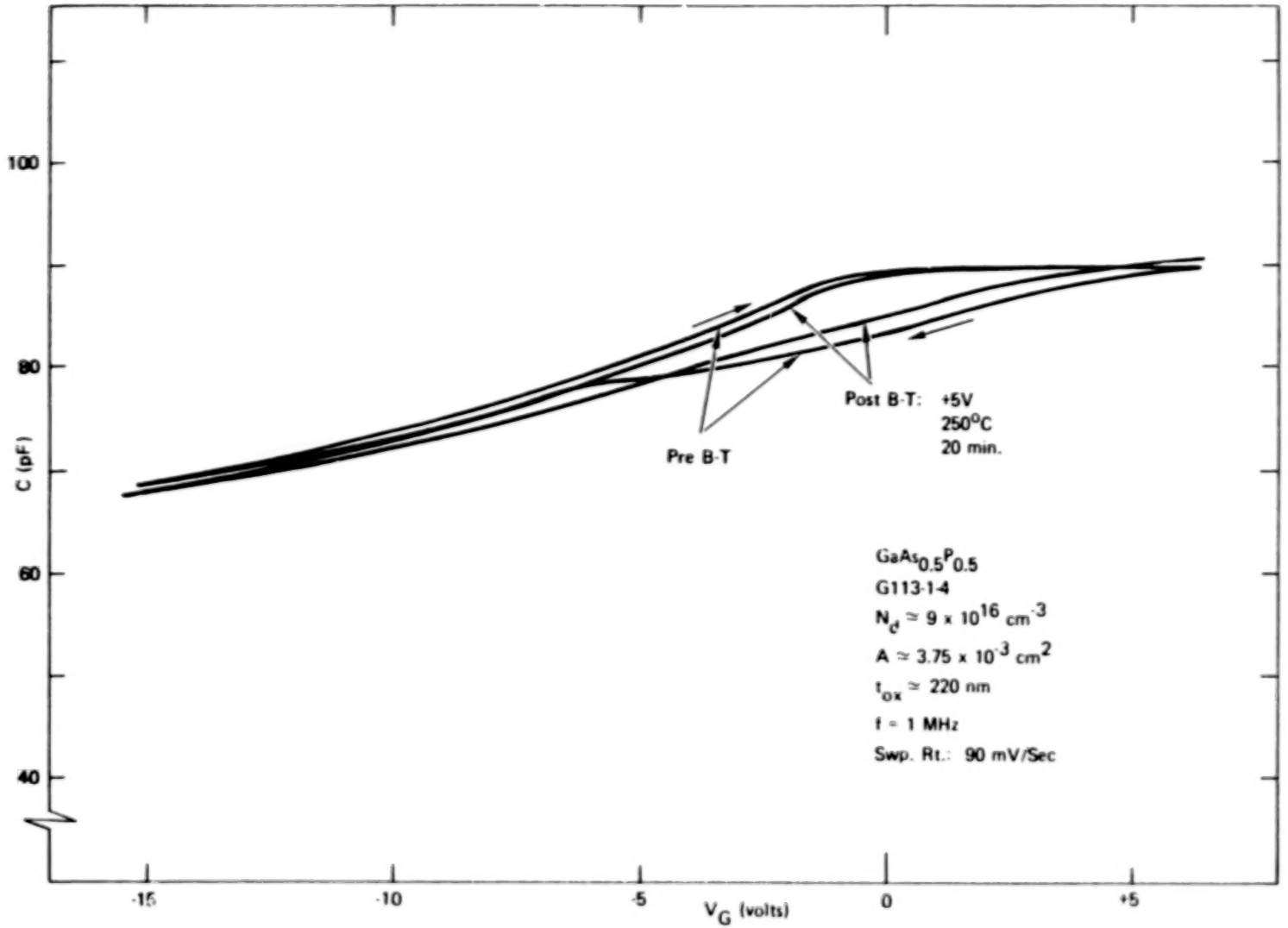

Figure 29. $GaAs_{0.5}P_{0.5}$ MIS C-V Characteristic

SECTION VI

SUMMARY AND CONCLUDING REMARKS

This section summarizes the major results of this program and some comments are then made regarding the usefulness of the dielectric fabrication processes and analytical techniques used in this work to the GaAs/$GaAs_{1-x}P_x$ technology, in particular, and III-V MOS technology, in general.

MIS Capacitor Electrical Characteristics and Dielectric Composition

The results of this program have shown that the thermal oxidation of the alloy $GaAs_{1-x}P_x$ produces films which are generally arsenic-deficient. The ion microprobe profiles indicate that phosphorus is incorporated into the oxide during growth. Although the IMMA cannot detect the presence of the gallium phosphate molecule, due to low ion sensitivity at this high molecular mass (amu 164 and 166 for $^{69}GaPO_4$ and $^{71}GaPO_4$, respectively), it is the most likely phosphorus-containing compound in the oxide. Recent results using x-ray photoelectron spectroscopy (Reference 18) indicate that $GaPO_4$ is the primary GaP thermal oxidation product, in agreement with early results (Reference 19). The application of XPS techniques to the oxides on $GaAs_{1-x}P_x$ should provide more definitive chemical bonding information.

The usefulness of the ion microprobe in examining the oxide composition is somewhat limited, in that it cannot provide unambiguous molecular and chemical information, due to the high masses of interest and masking by species of the same mass numbers which results from reactions of the primary ion beam with the sample (e.g., $^{71}GaAs^{18}O$ and $^{69}GaP^{16}O_4$ are both amu 164). However, the use of an inert beam would probably not result in any additional information due to decreased secondary ion yield. The IMMA measurements, in conjunction with other techniques, such as Auger and XPS could provide more detailed information which can be related to electrical characteristics. The present work has shown, however, that the ion microprobe is adequate for determining relative changes in the oxide composition resulting from fabrication variations and electrical stressing.

Comparison of both the electrical characteristics and the elemental oxide profiles demonstrates the important role of arsenic in determining the ultimate electrical properties of MIS devices utilizing this phosphorus-containing dielectric. High-temperature annealing results in arsenic loss from

the oxide surface. Annealing also changes the oxide electrical properties, resulting in reduced C-V hysteresis and slightly increased dielectric leakage current.

Argon annealing appears to substantially improve the interface properties, as evidenced by the reduced C-V hysteresis and decreased "apparent" interface state densities. However, analysis of the interface properties of these devices using techniques traditionally used for SiO_2-Si devices are probably inconclusive, as discussed earlier in this report and recently by Kohn and Hartnagel (Reference 20).

The chemical stability of the oxides under various stressing conditions used to assess the reliability of semiconductor devices is promising. Establishment of the basic chemical stability of the films will allow their further optimization for device application.

Based on the preliminary steam oxide results, it appears that lower-temperature oxidation and annealing processes are required to minimize or eliminate the arsenic loss and maintain stoichiometry in the films. The lower temperature steam oxidation processes should be investigated further. Such a low temperature thermal process, in conjunction with low temperature reactive (H_2) annealing may minimize both the arsenic loss from the oxide and the electron traps at the oxide-semiconductor interface region. In addition, other recent low-temperature oxidation processes, such as plasma or high pressure steam, may offer promising results.

Applications of $GaAs_{1-x}P_x$ Dielectric Development to Future III-V Compound Semiconductor Devices

Because of the wide interest in the many possible device applications of binary, ternary, and quaternary III-V compound semiconductors, it is natural to examine the usefulness of the results of this program to future device development.

The importance of arsenic in determining oxide electrical properites has been shown previously for films grown on gallium arsenide. The present work has shown that the presence of an additional element available for reaction during the oxidation process can result in a thermally grown oxide with dielectric properties which are somewhat improved over those of thermal

oxides on GaAs using the same open tube growth procedures. However, the numerous and competing oxidation reactions still result in films with less than optimum characteristics.

A recent systematic study of the low-temperature thermal oxidation of binary III-V compounds (Reference 21) has indicated that the phosphate-oxide grown on GaP is the most promising, because it is oxidized perfectly (i.e., stoichiometric). However, the arsenides (GaAs) and antimonides (GaSb and InSb) had a non-oxidized group V layer at the oxide-semiconductor interface.

With ternary and quaternary III-V compounds the situation is complicated because of the additional oxidation products which are possible. The desirability of forming amorphous layers to obtain a dielectric with good electrical properties requires knowledge and control of the chemical bonding between the compounds which form during growth. Knowledge of the growth kinetics and chemistry requires further study, as does the development of other experimental techniques for forming the oxides. Controlling the volatile reaction products, such as As_2O_3, by using lower temperature processes is probably a key to controlling the growth kinetics and obtaining satisfactory electrical properties for III-V compound MOS devices.

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16. Abstract

This report presents the results of a program to investigate the electrical properties and chemical stability of dielectrics thermally grown on $GaAs_{1-x}P_x$. Oxides were thermally grown on $GaAs_{1-x}P_x$, of various mole fraction, x, using dry oxygen or steam at various temperatures.

The elemental composition with depth into the oxide films was examined using secondary ion mass spectrometry. Results indicate that the layers are arsenic-deficient through the bulk of the oxide and arsenic-rich near both the oxide surface and the oxide-semiconductor interface region. Phosphorus is incorporated into the oxide in an approximately uniform manner.

MIS capacitor structures exhibited deep-depletion characteristics and hysteresis indicative of electron trapping at the oxide-semiconductor interface. Post-oxidation annealing of the films in argon or nitrogen generally results in slightly increased dielectric leakage currents and decreased C-V hysteresis effects, and is associated with arsenic loss at the oxide surface.

The results of bias-temperature stress experiments indicate that the major instability effects are due to changes in the electron trapping behavior. No changes were observed in the elemental profiles following electrical stressing, indicating that the grown films are chemically stable under device operating conditions.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Gallium Arsenide-Phosphide Oxidation MOS Capacitors Capacitance-Voltage Characteristics Ion Microprobe Analysis	Unlimited - Unclassified Subject Category 76

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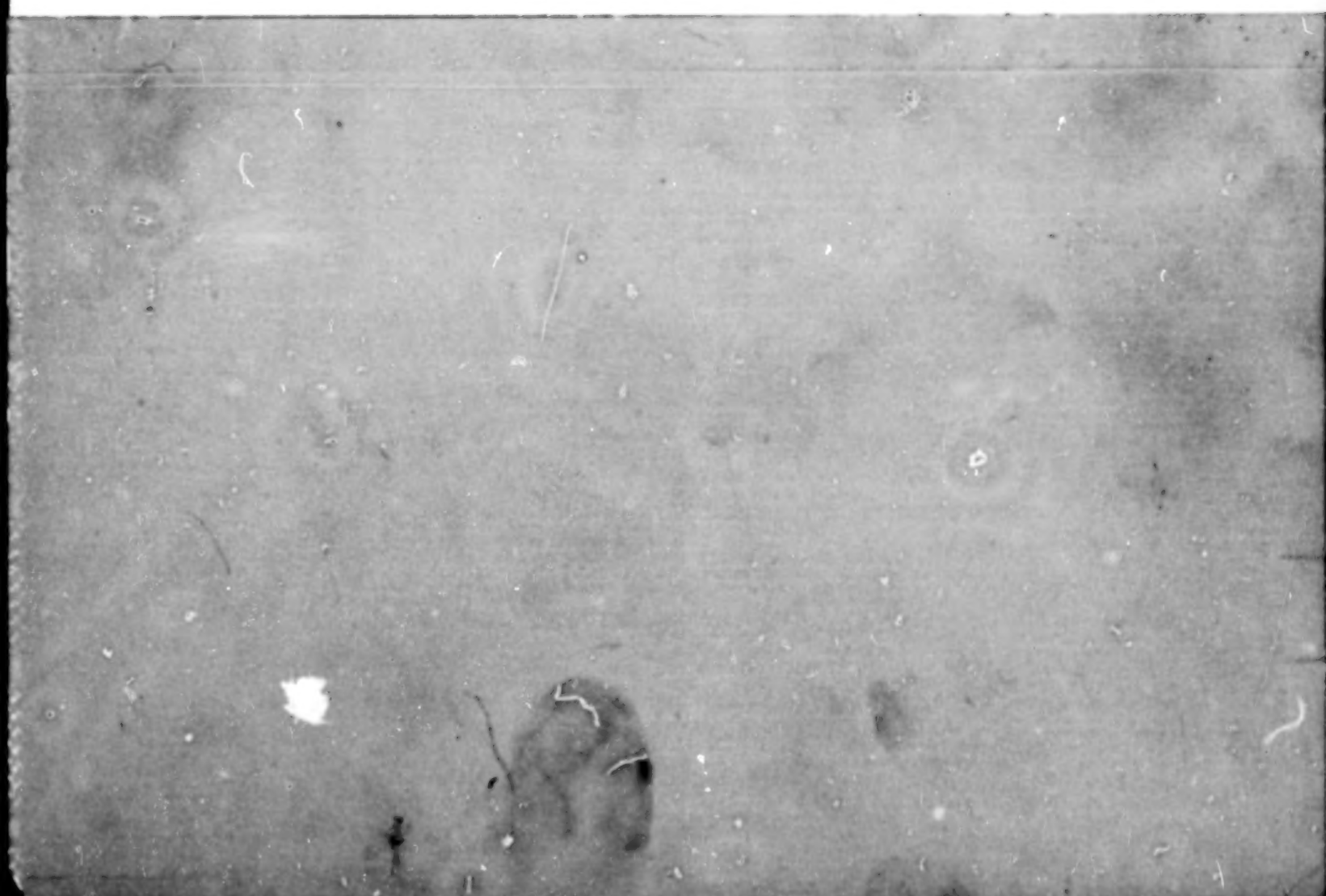

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